THE UNIVERSITY OF ALBERTA

THE DESIGN OF A POWER OUTPUT OPERATIONAL AMPLIFIER FOR MEASURING [illegible] [illegible] POTENTIALS.

BY

[illegible] L. [illegible]

A THESIS SUBMITTED TO THE FACULTY OF GRADUATE
STUDIES IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF MASTER OF SCIENCE

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON ALBERTA
APRIL 1965

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THE DESIGN OF A FIELD EFFECT TRANSISTOR AMPLIFIER FOR MEASURING BIO-ELECTRICAL ACTION POTENTIALS.

BY

ROBERT L. TUCKER

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled The Design of a Field Effect Transistor Amplifier for Measuring Bio-Electrical Action Potentials submitted by Robert L. Tucker in partial fulfillment of the requirements for the degree of Master of Science.

ABSTRACT

In the measurement of bio-electrical action potentials present on nerve fibres it is necessary to use an amplifier with a very high input impedance and low input current in order to obtain accurate results and avoid damage to the fibre. Since the micropipette probe through which connection is made to the fibre has an inherently high resistance and the signal being measured is small, the amplifier must also have a low noise figure. In the past these requirements have been met by using an electrometer tube as the input stage of the amplifier. In this thesis a solid state amplifier is designed using a field effect transistor in the input stage. It was also necessary to design a conventional noise amplifier in order to study the noise characteristics of the FET's and the completed circuit. As a final test on the bio-electrical amplifier a measurement was made of the action potential present in the sartorious muscle of a frog.

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CHAPTER I

Bio-Electrical Action Potential Amplifier Requirements

1.1 General

Many of the functions of the human body are instigated by electrical pulses. These pulses are transmitted through the body by means of a complex nerve system. In order to understand more about these nerve systems, the potentials present on them may be observed. This is not, however, as simple as it may appear. The main difficulties may be summarized as follows:

a) It is difficult to make an electrical connection to a nerve fibre without damaging it.

b) The nerve fibre is quite sensitive to electrical stimulation from the connected measuring device.

c) The shape and magnitude of the pulse is not easily reproduced without the use of an amplifier with a wide bandwidth.

In this chapter we will discuss these points in more detail in order to obtain the requirements which must be met by any amplifier used to measure these pulses. Once these requirements have been established, methods previously used for meeting them, as well as proposed changes to these methods, will be discussed.

1.2 Action Potentials

A nerve fibre in its normal condition will be at a negative "rest potential" of approximately 100 mv. When

a positive potential is applied to this fibre, the potential at this point will gradually rise until some "threshold" voltage is reached. At this time, the action will become self sustaining and produce a 150 to 200 mv. pulse with a rise time of approximately 100 micro-seconds. The pulse will then begin to fall at a somewhat slower rate back to the initial rest potential. The fall time will normally be about 500 micro-seconds although the rest potential is not reached for 2-3 seconds. A typical waveform is shown in figure 1-1.

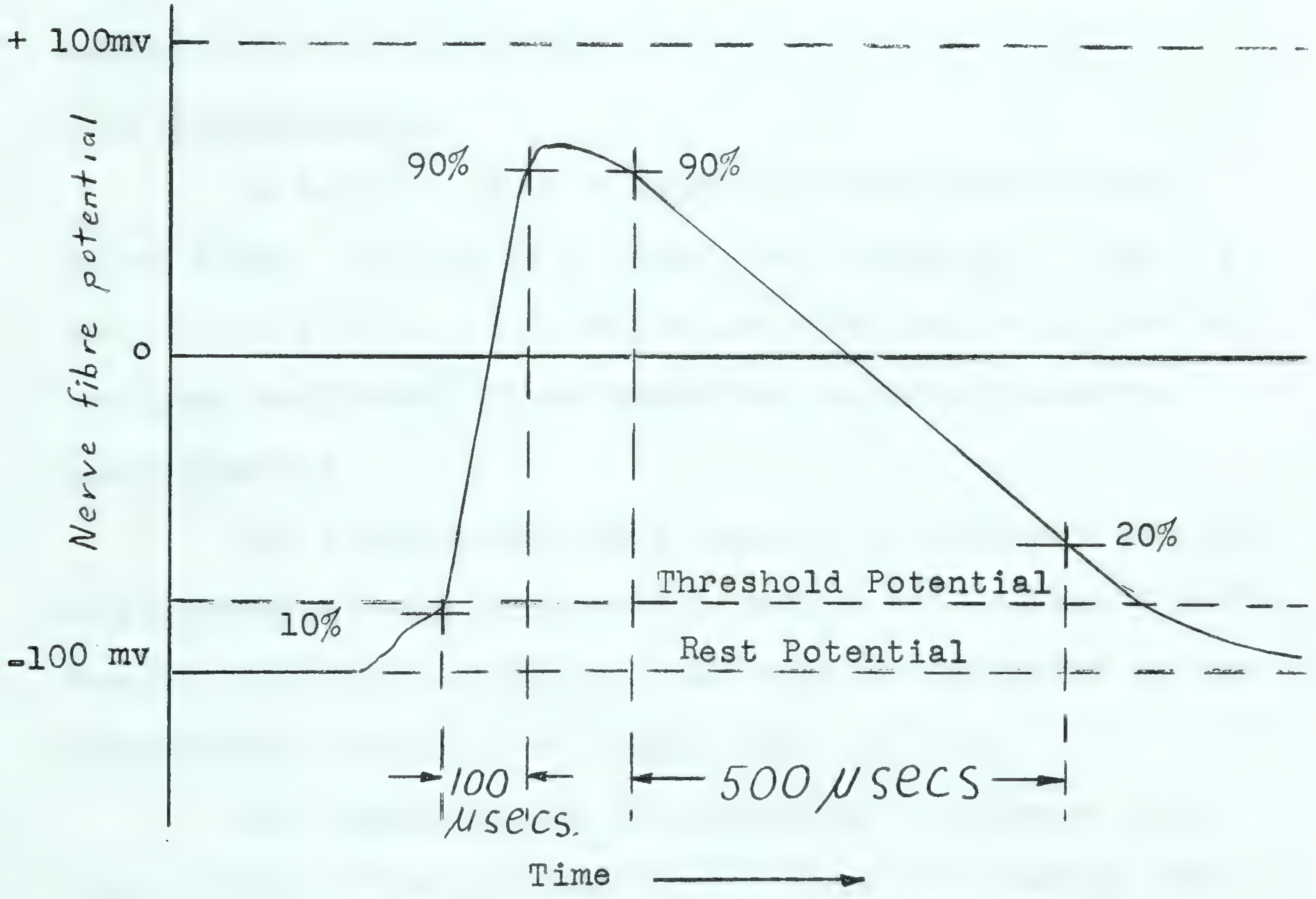


figure 1-1 Action Potential Waveform

This signal is then propagated along the nerve in a complicated and not completely understood manner to the point where measurements are to be made.

A rise time of 100 micro-seconds corresponds to a frequency response of approximately 3kc, but in order to accurately reproduce this rise time an amplifier having a frequency response of several times this value is required. According to Guld,(5) with a critically damped response, the error in the rising phase of a 100 mv. pulse can be kept below 5 mv. at half amplitude if the amplifier has a 30 kc bandwidth. It would therefore be desireable to have a bandwidth of at least 30kc.

1.3. Micropipette

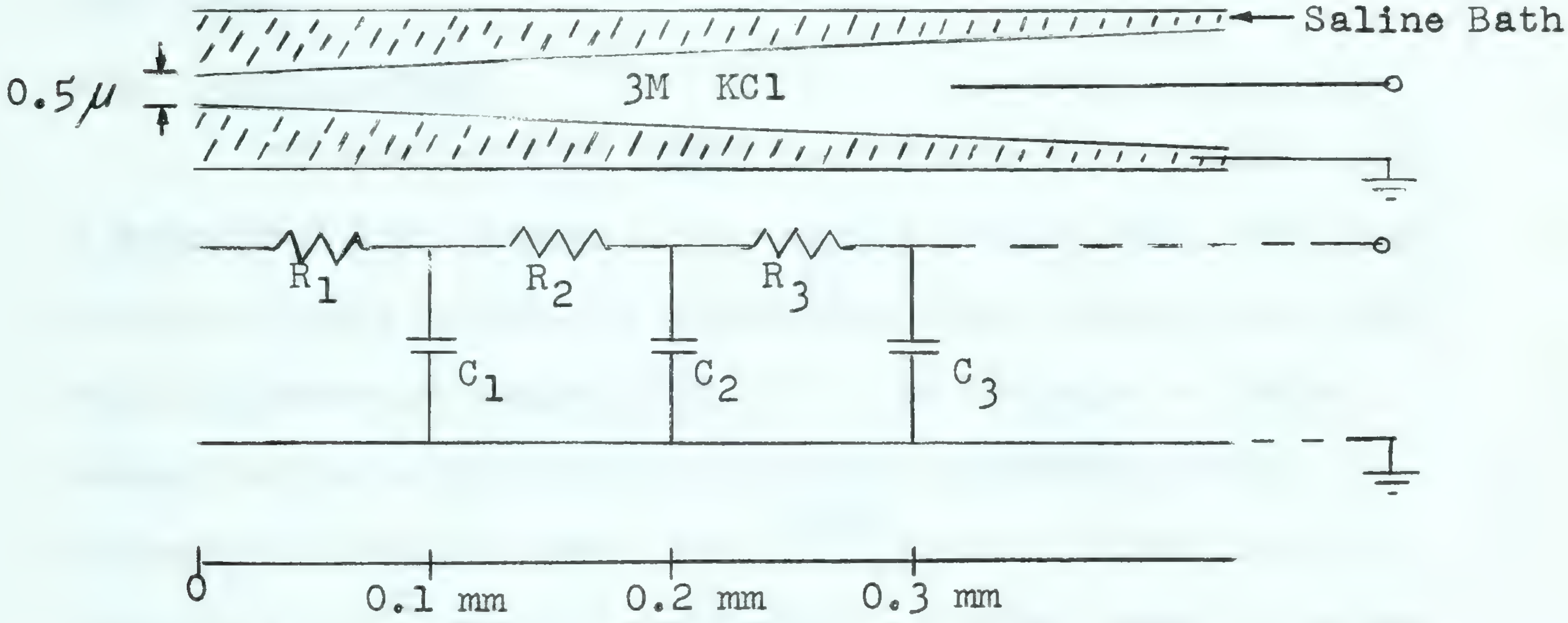
In order to make electrical connection to the nerve fibre, the use of a glass tube drawn to a fine tip and filled with an electrolyte has come into wide use in the past ten years.(2) These tubes are commonly known as micropipettes.

The tip diameter of a useful micropipette is about 0.5 microns and the pipette is usually filled with 3 M KCl. Due to this tip restriction, the lineal resistance of the micropipette becomes very large near the tip.

The normal method of measuring potentials on a nerve fibre is to submerge the specimen in a saline bath in order to prevent its dehydration. This bath also acts as

the ground connection to the nerve, and the micropipette must pass through it before reaching the fibre. This means that a distributed capacitance between the grounded bath and the electrolyte inside the pipette will exist.

For our purposes an approximate lumped equivalent circuit can be used to represent these distributed paramaters. The variation of these values with micropipette penetration is shown in figure 1-2, as well as the proposed equivalent circuit.



$R_1 >> R_2 >> R_3$ -------

or as a further simplification

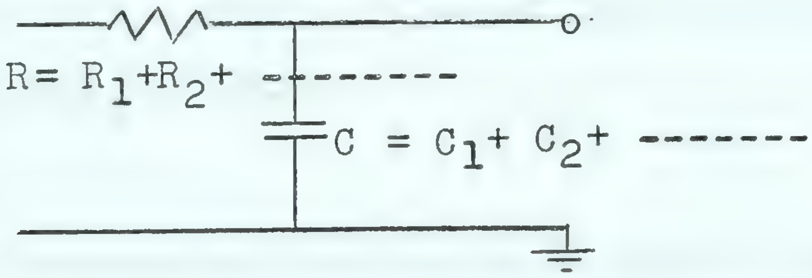


figure 1-2 Micropipette Equivalent Circuit

The values of the tip resistances are extremely variable due to the variability of the methods of preparing micropipettes, but the lumped total R will normally be between 5 and 50 megohms, and C will normally be 1 to 2 picofarads.

In order to couple the signal from the nerve fibre to the amplifier with a 1% accuracy, it will therefore be necessary to have an input resistance of the order of 10^{10} ohms.

1.4. Input Current

If a current is applied to the cell, it will cause a potential drop across the membrane of the cell. The magnitude of this potential depends upon the size of the cell and its membrane resistivity. If this voltage is large enough to raise the potential to the threshold level, a pulse will be generated. Most (1)(3) sources agree that a current of 10^{-10} amps is sufficient in some cases to raise the potential to this level. It therefore appears that the input current of the amplifier should be less than 10^{-11} amps, or preferably 10^{-12} amps, to avoid the possibility of this current producing a pulse.

1.5. Drift

Since it is usually desireable to record the rest potential, a direct coupled amplifier is required. With direct coupled amplifiers, some problem is encountered with output voltage drift. Since most tests are completed in an

hour or less, an output voltage drift of no more than 1 mv per hour, referred to the input, would appear reasonable. Since the amplifier will normally be used in a fairly constant temperature room, with a temperature variation of no more than 3° C/ hour, a drift with temperature of less than 0.3 mv./ °C is required. These two drifts must be considered as independent requirements, since drift with time may occur at a constant temperature due to power supply variations.

1.6. Noise

For an amplifier with a 30 kc bandwidth and a 50 megohm source impedance, a noise voltage of about 0.15 mv. will be generated. In order to observe a 1 mv. change in the action potential, or rest potential, it would be preferrable to limit the noise to 0.30 mv. if possible. This corresponds to a noise factor of 4, or a noise figure of 6 db.

1.7. Summary of Requirements

The requirements of the amplifier can be summarized as:

a) Frequency response	dc to 30 kc
b) Input resistance	$> 10^{10}$ ohms
c) Stable input current	$< 10^{-11}$ amps
d) Drift	$<$ 0.3 mv./ °C.
	$<$ 1.0 mv./ hr.
e) Noise figure (0-30 kc)	$<$ 6 db

1.8. Previous Amplifiers

These requirements have been met in the past by using an electrometer tube for the input stage. These tubes have a very small input current when operated at reduced potentials, as well as a very high input impedance.

In order to reduce input capacitance, these tubes were operated in a cathode follower configuration, with the shield around the input lead connected to the cathode. This reduced the grid-to-cathode capacitance Cgk to:

$$C'_{gk} = C_{gk}(1-A) \qquad \text{where } A = \text{grid-to-cathode gain}$$

This process is commonly referred to as capacitance neutralization.

The next improvement to the input stage was a circuit in which the plate voltage also followed the input signal. This effectively reduced the capacitance from grid to plate.

The final step in the evolution of this field of amplifiers was to feed an in-phase signal into the grid through a small capacitor. This gave an effective negative capacitance to the grid, which could be adjusted to equal the input capacitance present. This was a big step since the input capacitance could be expected to be different for each setup. It also gave a simple method of adjusting the system damping for optimum reproduction.

Although these circuits all worked well, they were

subject to microphonics and could not be reduced in size for special applications.

1.9. Proposed Design

In order to eliminate these microphonics and prepare a circuit which could be reduced in size, the design proposed will use semiconductor devices for all active stages. This was impossible until the recent advent of the field-effect transistor with its high input impedance and low noise figure.

The lessons of the past will, however, be observed by applying both negative capacitance and capacitance neutralization.

CHAPTER II

NOISE AMPLIFIER DESIGN

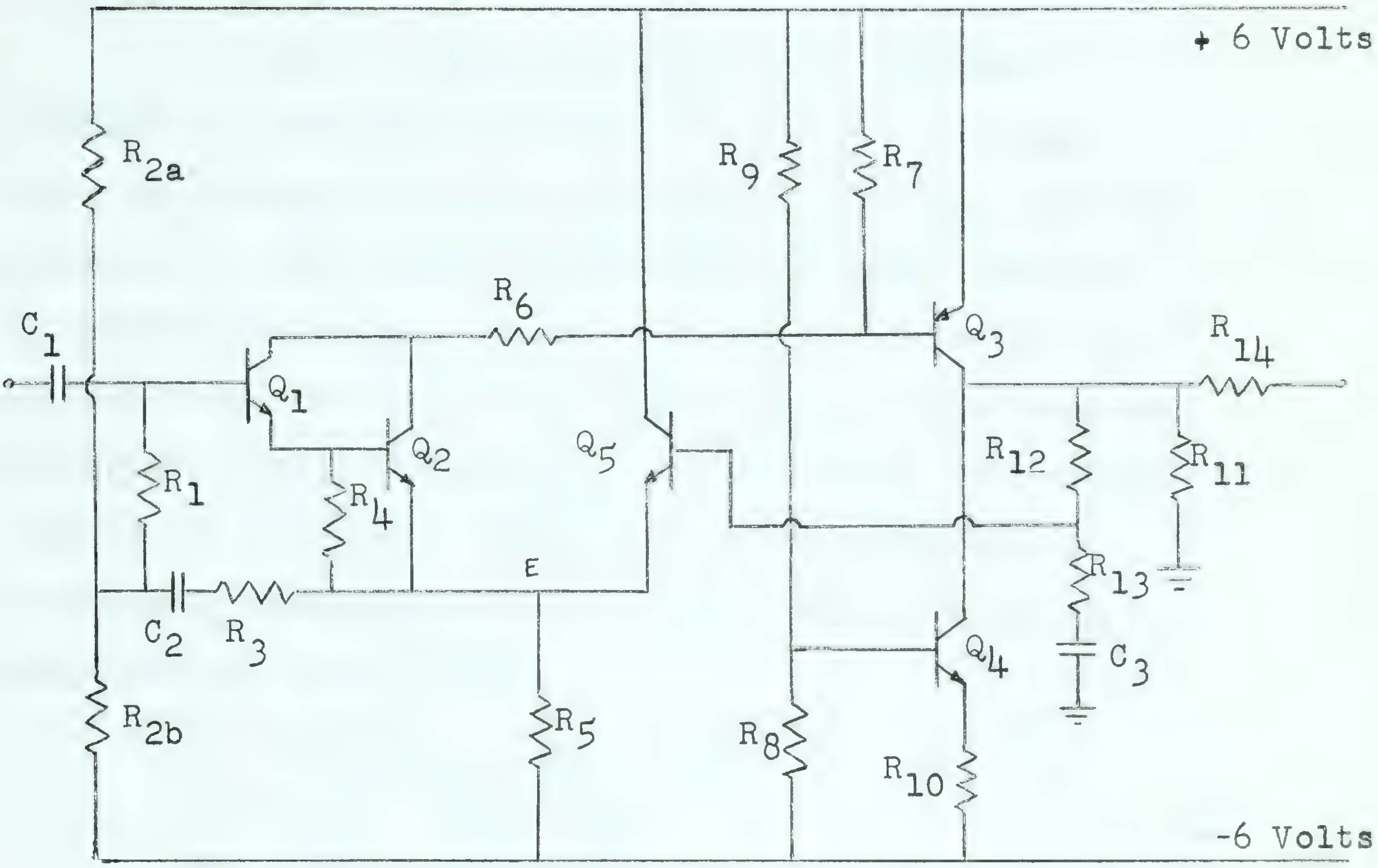
2.1. Requirements

Since it was desired to make a very low noise biological amplifier, some means of measuring the noise and comparing the noise of different components was required. Any accurate measuring technique which could be chosen was found to require an amplifier with a gain of about 1000 and a frequency response at least as wide as that of the biological amplifier.

It was decided to measure noise as a voltage source rather than a power or current source, due to the ease and accuracy of making voltage measurements. (This is, however, still a method of measuring noise power). This method of measurement requires an amplifier with a high input impedance. Since the output impedance of a field effect transistor is usually about 100 K ohms, an input impedance of about 10 megohms was considered sufficient.

2.2. General Circuit

The circuit as finally evolved consisted of a bootstrapped Darlington connected input stage as one leg of a differential amplifier. The output of this stage was then fed to a high gain second stage. The feedback loop was closed by feeding a portion of the output into the base of the transistor forming the second leg of the differential stage. The complete circuit is shown in figure 2-1.



R_1 = 1 Meg.

R_{2a} = 3.26 Meg.

R_{2b} = 4 Meg.

R_3 = 39K

R_4 = 680K

R_5 = 27K

R_6 = 1K

R_7 = 6.8K

R_8 = 1K

R_9 = 10K

R_{10} = 1K

R_{11} = 100K

R_{12} = 1 Meg.

R_{13} = 820 Ω

R_{14} = 1K

C_1 = .012 μf

C_2 = 0.1 μf

C_3 = 300 μf

Q_1 = TI415

Q_2 = TI415

Q_3 = 2N3251

Q_4 = 2N1304

Q_5 = TI415

figure 2-1 Noise Amplifier Circuit Diagram

2.3. Input Stage

In order to obtain the high input impedance required, a Darlington compound was used in the input stage in a common emitter connection with a large emitter resistor. In this type of connection the input impedance is approximately $h_{fe}R_E$, where R_E is the resistor in the emitter lead, and h_{fe} is the current gain of the compound. Therefore, a high value of h_{fe} is desireable. The performance of the Darlington connection can be described by considering the compound as a single transistor having h-paramaters as shown below:

$$h^*_{fe} = h_{fe1}h'_{fe2} + h_{fe1} + h'_{fe2}$$
$$h^*_{ib} = h_{ib2} + h_{ib1} / h'_{fe2}$$
$$h^*_{ob} = h_{ob1} + h_{ob2} / h_{fe1}$$
$$h^*_{rb} = h_{rb1} + h_{rb2}$$

Where

$$h'_{fe2} = \frac{h_{fe2}R_4}{h_{fe2}h_{ib2} + R_4}$$

Noise is also an important characteristic of this stage since the noise performance of an amplifier is normally limited by the noise performance of the first stage. Nielson(7) has shown that for large source impedances the best noise performance is obtained by using high current gain devices operating at very low collector current levels.

With these considerations in mind it was decided to operate Q_1 at about one microamp collector current, and Q_2 at 100 microamps, with both Q_1 and Q_2 being high current gain TI415 Silicon NPN transistors. The input impedance

and noise performance of the amplifier will be discussed in a later section after the closed loop performance of the amplifier has been calculated.

2.4. Second Stage

The voltage gain of the first stage from base to collector will be quite small, since its main function is to provide an impedance transformation and a high input impedance. Therefore, a high gain second stage is required. This was obtained by operating Q_3 in a common emitter stage and using Q_4 connected as a constant current source for the A.C. load impedance. The gain is reduced from the maximum possible for this arrangement by shunting Q_4 with R_{11}, a 100 K resistor. This reduces the effect of the output loading on the gain of the circuit. In order to obtain high gain without limiting the frequency response too severely a 2N3251 Silicon PNP transistor was used for Q_3. A 2N1304 germanium transistor was satisfactory for Q_4.

We may now calculate the input impedance and voltage gain of this stage using well known equations.

$$Z_{in2} = h_{fe}h_{ib}\,\frac{1 + \left(\dfrac{h_{rb}}{h_{ib}} + h_{ob}\right) R_L}{1 + h_{fe}h_{ob}R_L} \,/\!/\!/\, R_7$$

where R_L = 100 K ohms and the h-paramaters are those of Q_3.

Therefore: $Z_{in2} = 5.8\text{K} /\!/ R_7 = 3.12\text{K}$

The voltage gain is:

$$A_{v2} = \frac{R_L}{h_{ib}}\,\frac{1}{1 + \left(\dfrac{h_{rb}}{h_{ib}} + h_{ob}\right) R_L}$$

$$= -1590$$

2.5. Differential Stage

In the circuit of figure 2-1, Q_1 and Q_2 form one leg of a differential amplifier and Q_5 forms the second leg with R_5 supplying a fairly constant current to the stage. The main function of the differential stage, in this case, is to provide a high impedance point(i.e. the base of Q_5) in which to close the final feedback loop. In order to obtain balanced operation as well as a low noise performance, a third high gain TI415 transistor, operated at 100 microamps, was used for Q_5.

For calculations we may consider the input stage as a common emitter with an unbypassed emitter resistor approximately equal to h_{ib} of Q_5. Under these conditions the voltage gain of the first stage can be calculated as:

$$A_{v1} = \frac{-G}{1 + g}$$

where $G \simeq \dfrac{Z_{in2}}{h_{ib5}} = 11.5$

and $g \simeq \dfrac{h_{ib}^{*}}{h_{ib5}} = 1.51$

Therefore $A_{v1} \simeq -4.6$

2.6 Closed Loop Response

The total open loop gain of this amplifier will be:

$$A_{vo} = A_{v1} A_{v2} = 7300$$

When the loop is closed by feeding a portion (β) of the output to the base of Q_5, a gain of close to 1000 is realized.

The feedback ratio is:

$$\beta = \frac{R_{13}}{R_{12} + R_{13}} = 0.82\text{x}10^{-3}$$

This value of β will hold until the reactance of C_3 approaches 820 ohms. The corner frequency of this rise was set at 0.65 cycles/ second by making C_3 a 300μf capacitor. The closed loop gain will be:

$$A_{vc} = \frac{A_{vo}}{1 + \beta A_{vo}} = 1040$$

At this point the closed loop gain from the input to the point E of figure 2-1 can be calculated from the equivalent circuit of figure 2-2, where h^*_{ib} is the equivalent h_{ib} of the Darlington compound connection as given in section 2.3, and $V_2 = V_1 A_{vc} \beta$

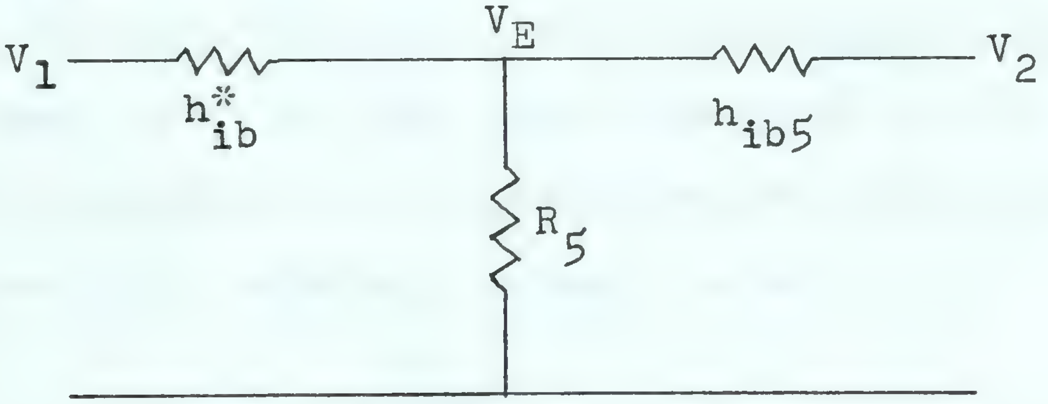


Figure 2-2 Differential Amplifier Equivalent Circuit

If we write node equations for this circuit we find that the gain to the point E is:

$$A_{VE} = \frac{V_E}{V_1} = 0.905$$

We may also calculate resistance Z'_{in1} seen looking into the base of Q_1. With the loop closed we can consider the differential circuit to be a single transistor stage loaded by Z_{in_2} and with an equivalent emitter resistor Z_{eq}. The closed loop gain of the first stage is:

$$A_{v1c} = \frac{A_{vc}}{A_{v2}} = -0.654$$

Then $Z_{eq} = \dfrac{-Z_{in2}}{A_{v1c}} - h^{*}_{ib} = 4.73K$

and $G_{eq} = Z_{in2}/ Z_{eq} = 0.66$ $\qquad$ $g_{eq} = h^{*}_{ib}/ Z_{eq} = .0086$

The input resistance of this stage is given by:

$$Z'_{in1} = (1 + g_{eq}) \left[h^{*}_{fe} Z_{eq} /\!/ \frac{1}{(1 + G_{eq}) h_{ob1}} \right] \simeq 30 \text{ Megohms}$$

2.7. Bootstrapped Bias Network

The main function of the bootstrapped bias network, in this case, is to set the input impedance to the level required. The impedance of the bootstrapped resistance R_1 as seen at the input terminal, appears to be:

$$Z_{bias} = \frac{R_1}{1 - A}$$

where $A = \dfrac{R_2}{R_2 + R_3} A_{VE} = 0.886$

and $R_2 = R_{2a} /\!/ R_{2b}$

The input impedance of the amplifier can therefore be calcul-

ated as:

$$Z_{in} = Z'_{in1} // \frac{R_1}{1 - A} = 6.8 \text{ Megohms}$$

This value was considered to be sufficiently close to the requirement of about 10 Meg. given in section 2-1.

In order to calculate the low frequency performance of the input stage, Edwards(4) has shown that the bootstrapped network shown in figure 2-3 can be described as an operational amplifier with feedback as shown in figure 2-4.

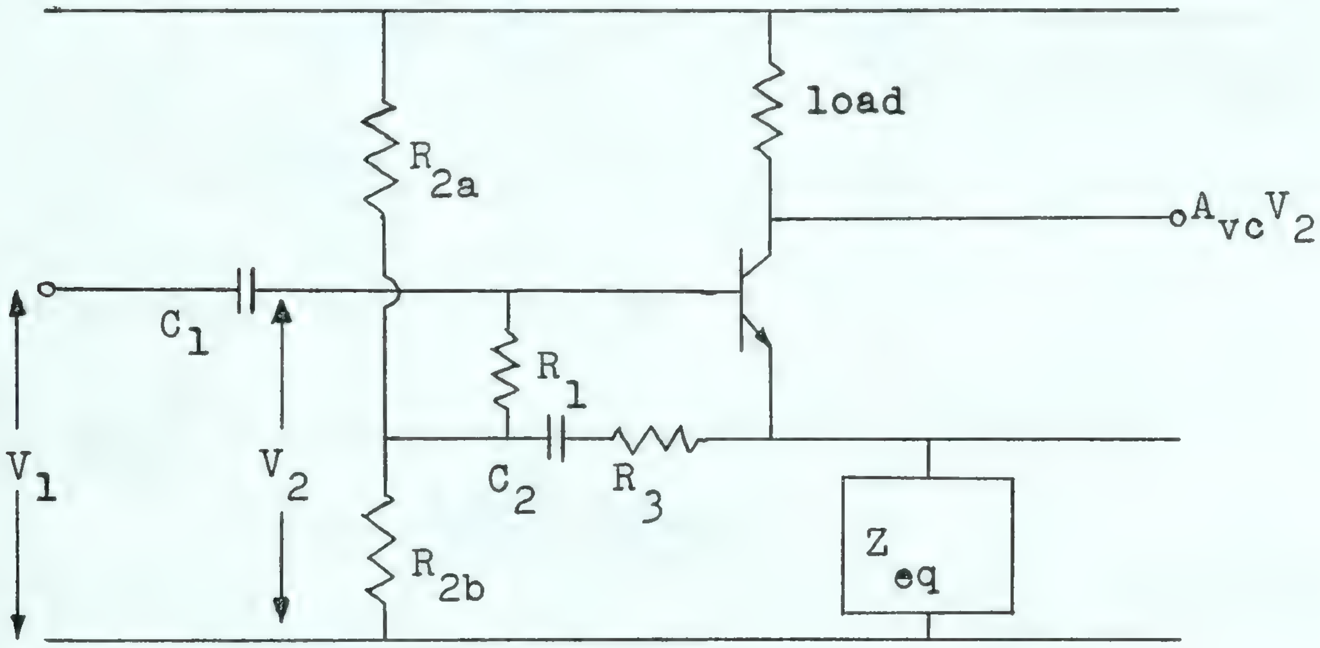


figure 2-3 Bootstrapped Bias Stage.

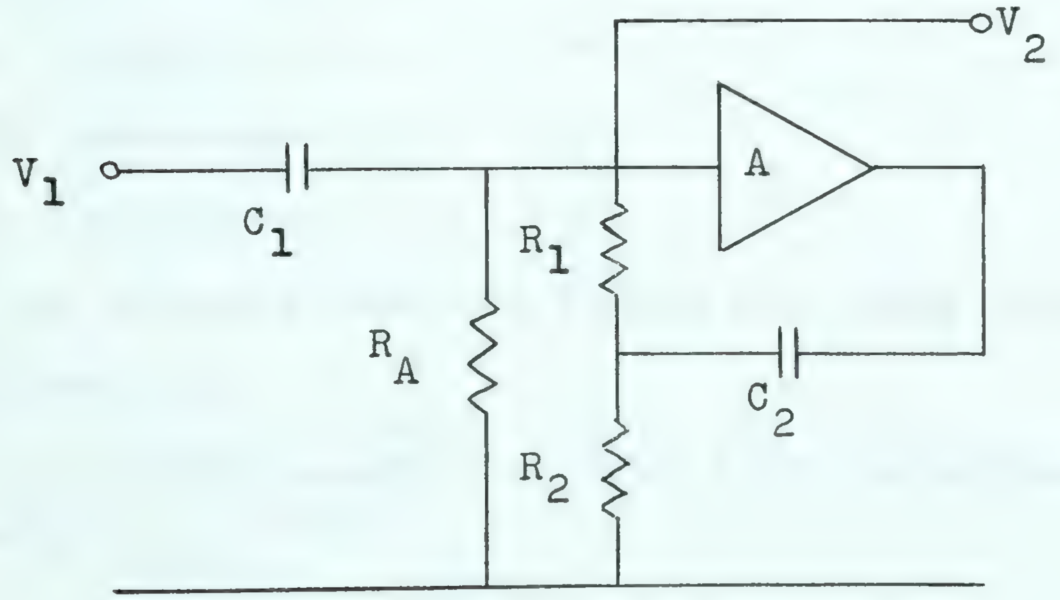


figure 2-4 Equivalent Circuit of Bootstrapped Bias Stage.

The transfer function of this system is :

$$H[p] = \frac{V_2}{V_1} = \frac{p^2 + 2\zeta_1 p}{p^2 + 2\zeta p + 1}$$

where $p = T_o s = \frac{s}{\omega_o}$

$$T_o = \tfrac{1}{2} R_c \sqrt{C_1 C_2}$$

$$R_c = R_1 + R_2$$

$$\zeta_1 = \sqrt{C_1/C_2}$$

$$\zeta = \tfrac{1}{2}\sqrt{\frac{1-\alpha}{\alpha}\frac{C_2}{C_1}}\left[1 - A + \alpha\frac{R_c}{R_A} + \frac{C_1}{(1-\alpha)C_2}\right]$$

$$\alpha = \frac{R_1}{R_c}$$

It is also shown that if $p = jU$

$$\left|H\ [jU]\right|^2 = \frac{1}{1 + \dfrac{2\gamma U^2 + 1}{U^4 + 4\zeta_1^{\,2} U^2}}$$

Where $\gamma = 2\zeta^2 - 2\zeta_1^{\,2} - 1$

And the system will be

a) Maximally flat if $\gamma = 0$

b) Underdamped if $\gamma < 0$

c) Overdamped if $\gamma > 0$

With the elements shown in figure 2-1 these values can be calculated as:

$T_o = 0.0992$ seconds, or $f_o = 1.62$ cycles/second

$\zeta = 0.776$

$\zeta_1 = 0.139$

$\gamma = + 0.152$

From these results we see that the input stage will have a slightly overdamped frequency response and a low-frequency cut-off of 1.62 cycles/second.

2.8. Summary and Experimental Results

The calculated and measured characteristics of the amplifier are summarized in table 2-1, and show a good agreement. The open loop and closed loop gains are plotted as a function of frequency in graph 2-1. The upper cut-off frequency of 42kc indicates a C_{ob} of Q_3 of about 4.5pf, which is a reasonable value for a 2N3251 transistor.

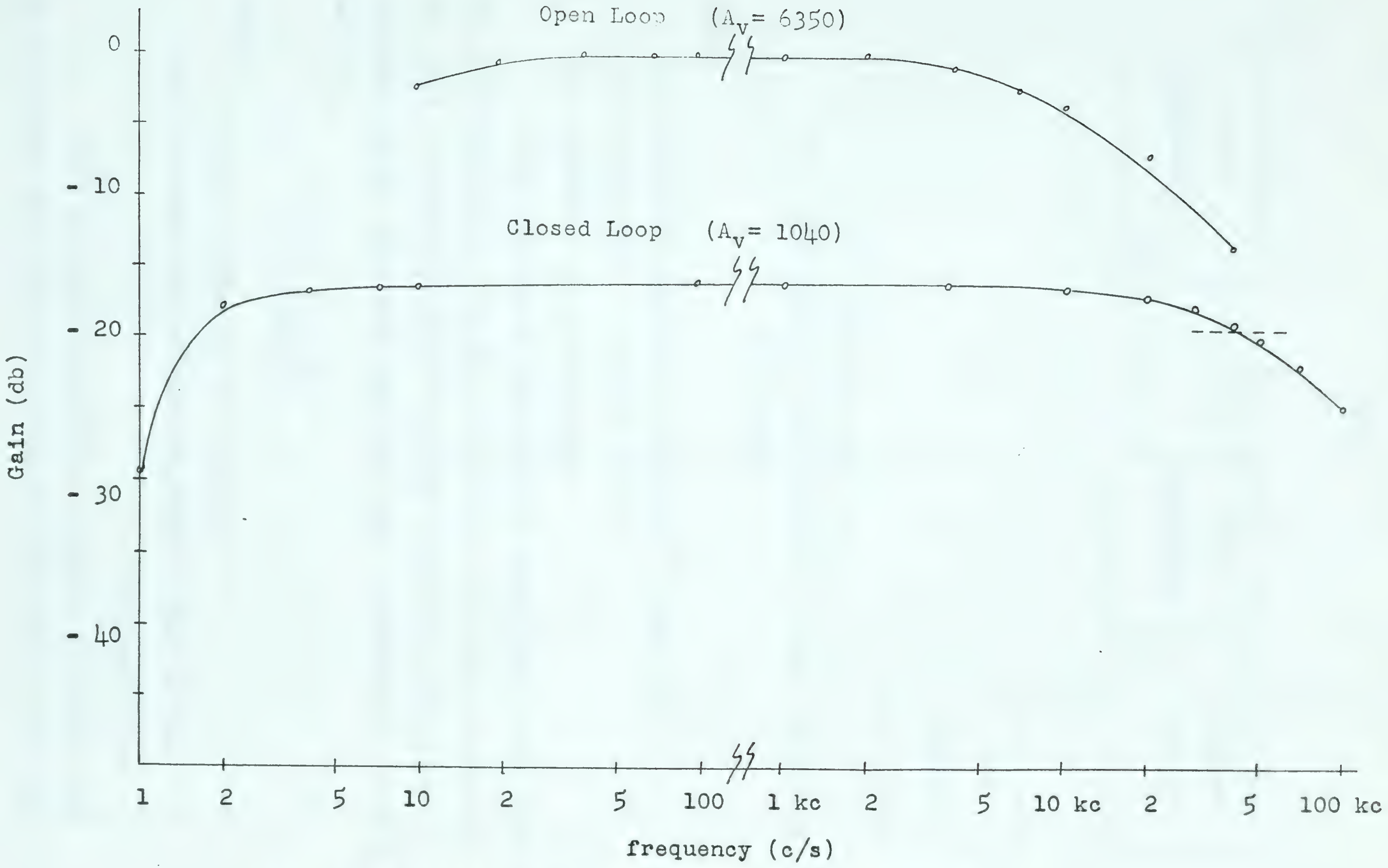
The input impedance of the amplifier was found to remain constant over the entire bandwidth at 7.4 megohms in parallel with 17 pf.

Table 2-1.

Characteristic	Theoretical	Measured
Open loop gain	7300	6500
Closed loop gain	1040	1040
Input impedance	6.8 Meg.	7.4 Meg.
Input capacitance		17 pf.
Upper cut-off frequency with R_s=0		42 kc
Lower cut-off frequency	1.62 cycles/sec.	1.7 cycles/sec.

2.9. Noise Performance

The noise performance of the amplifier was measured by means of the setup shown in figure 2-5.



Graph 2-1 Noise Amplifier Frequency Response with $R_s = 0$

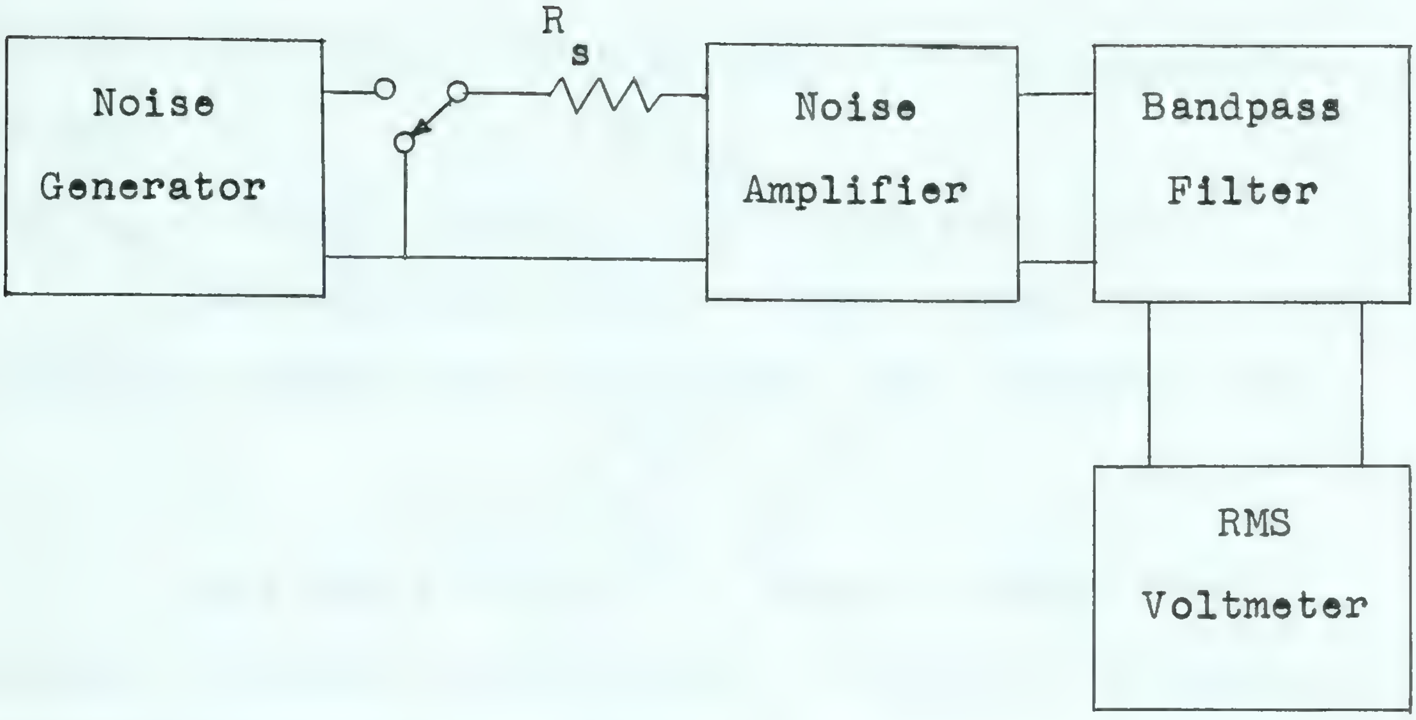


Figure 2-5 Noise Measurement Setup

The resistance R_s will generate a noise voltage of:

$$e_n^2 = 4kTR_sB$$

Where

k = Boltsmans constant = 1.374×10^{-23} joule/ °K

T = Temperature in degrees Kelvin

B = Bandwidth in cycles/second

With the switch connected to ground the noise voltage generated by R_s will be amplified by the noise amplifier and give a reading on the "true" RMS voltmeter. The value measured by the voltmeter when the input impedance Z_{in} is $>> R_s$ will be:

$$e^2_1 = e^2_n A_v^2 F$$

where

F = noise factor of the amplifier

A_v = voltage gain of the amplifier x gain of the bandpass filter.

When the noise generator is placed in series with R_s its output will also be present at the input to the ampli-

fier. The input due to this voltage, providing $Z_{in} \gg R_s$ will be:

$$e_2 = A_v e_{ng}$$

where e_{ng} = output voltage of the noise generator.

The total RMS output voltage, since there is no correlation between the two sources, will therefore be:

$$e_t = \sqrt{e_1^2 + e_2^2}$$

This means that if the output voltage with R_s connected to ground is increased 3 db when R_s is connected to the noise generator, then $e_1 = e_2$.

or: $$(e_n A_v)^2 F = (e_{ng} A_v)^2$$

and the noise factor is $F = \dfrac{e_{ng}^2}{e_n^2}$

The value of the noise factor found by this method can be converted to the more commonly used noise figure by a simple formula.

$$NF = 10 \log_{10} F$$

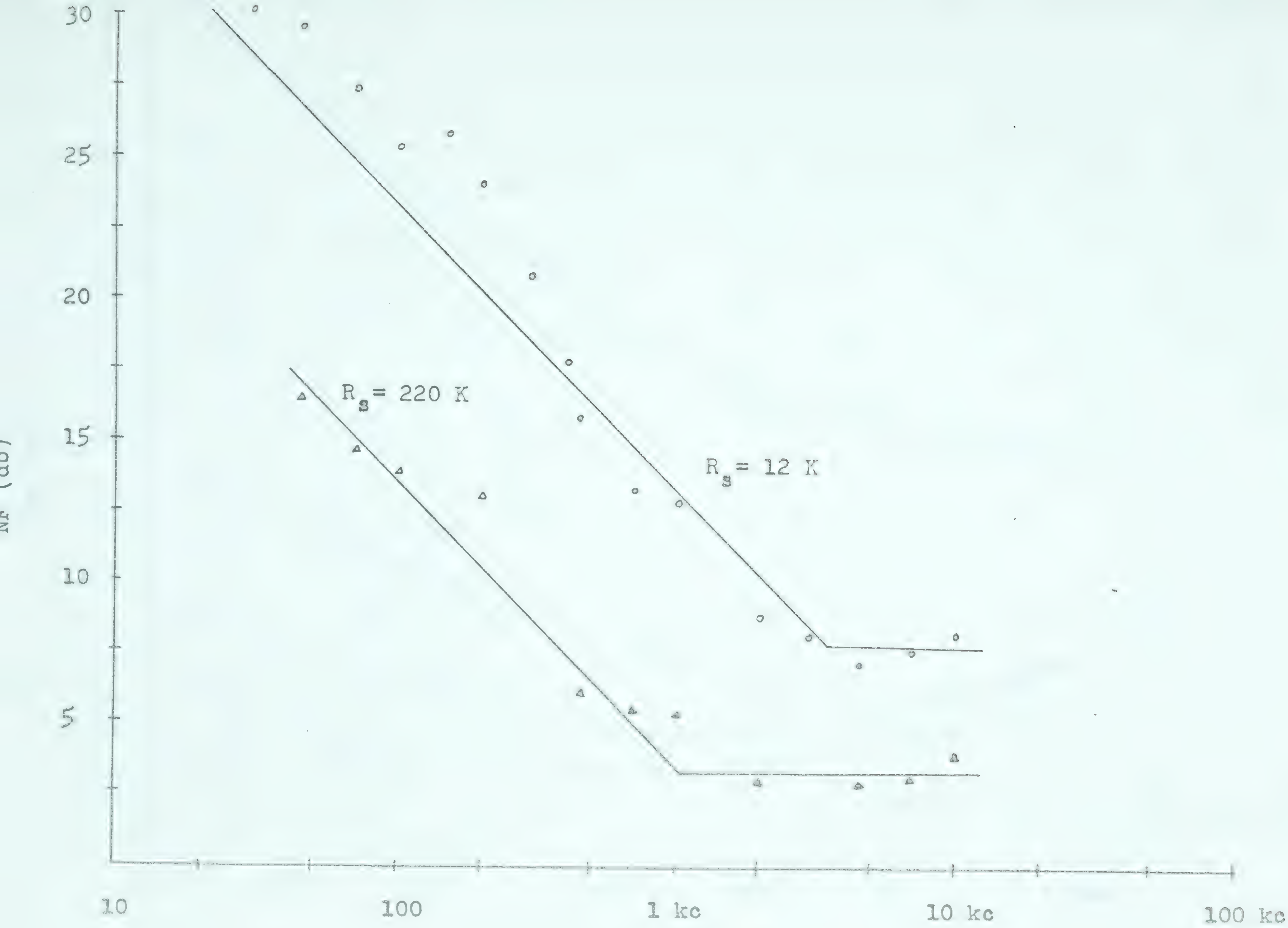
Since noise figure varies with frequency and with source impedance R_s, both of these variations were measured. The bandwidth was held at ± 10% or ± 20% of the center frequency by means of the bandpass filter.

The noise performance of the amplifier was found to be quite satisfactory as shown in graphs 2-2 and 2-3. With the source impedance set at the design center of 220k ohms, graph 2-2 shows that the high frequency noise figure was about 3 db, with $\frac{1}{f}$ noise predominating below 1kc. This graph also shows that the $\frac{1}{f}$ noise begins to predominate at

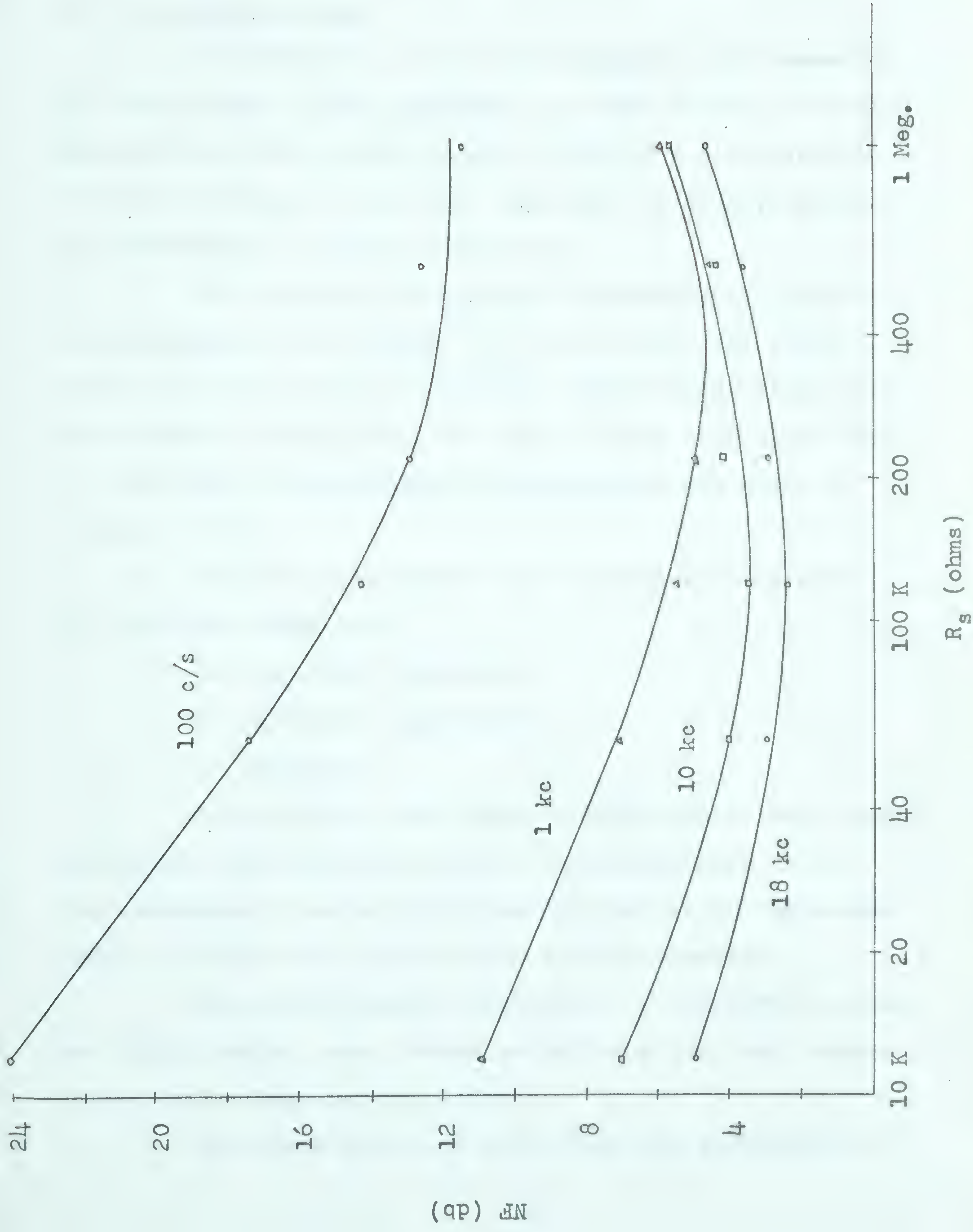
a higher frequency when the source impedance is lowered to 12 K. The accuracy of the measurements at low frequencies is greatly reduced from the ± 1 db tolerance found at frequencies above about 1 kc, due to the great difficulty involved in reading noise voltages at low frequencies.

In graph 2-3 the noise figure is shown to reach a broad minimum at source impedances of 100 K ohms to 200 K ohms for high frequencies, with the minimum shifting to greater than 400 K at 100 c/s. Since the majority of the frequency spectrum of the amplifier is above 1 kc, it is seen that the noise figure is optimized when the source impedance is close to the design center of 220 K.

Before making these tests, several different T1415 transistors were tried in the input stage, and the unit having the lowest noise figure was used. The noise figure appeared to be lowest with the highest gain units, as predicted by noise theory(7).



Graph 2-2 Variation of Noise Figure with Frequency



Graph 2-3 Variation of Noise Figure with Source Impedance

CHAPTER III

BIOLOGICAL AMPLIFIER DESIGN

3.1. Component Testing

In chapter I, several requirements were placed on the input stage of the amplifier. In order to help determine whether these requirements could be met by a field effect transistor stage, it was first necessary to closely analyze the performance of these transistors.

Low frequency admittance paramaters, or conductance paramaters, are usually used to describe the performance of a field effect transistor. Capacitance values are also stated in most cases. The small signal equivalent circuit as well as conversions to h-paramaters are given in Appendix I.

The main requirements on the device to be used for the input stage are:

1) high input impedance
2) low input capacitance
3) low noise

It was found that these characteristics were associated with low values of forward transconductance. Since transconductance can be multiplied by the use of compounded stages, this was not felt to be a serious drawback.

Several Siliconix transistors of the 2N2600 series and 2N2840 series, were chosen as having a low input capacitance, and a high input impedance.

The noise figure of these units as a function of

frequency and source impedance, was then measured, using the set-up of figure 3-1.

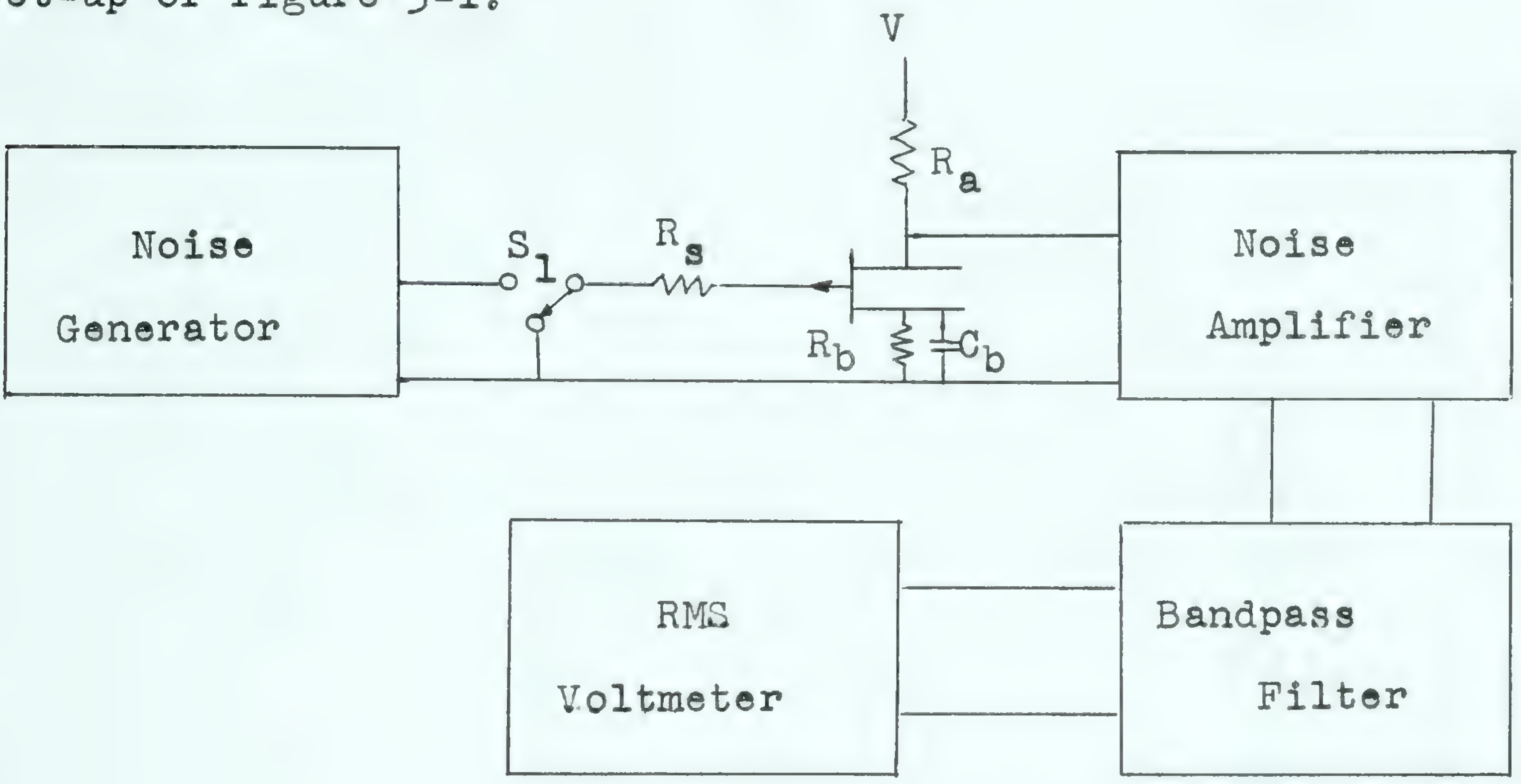


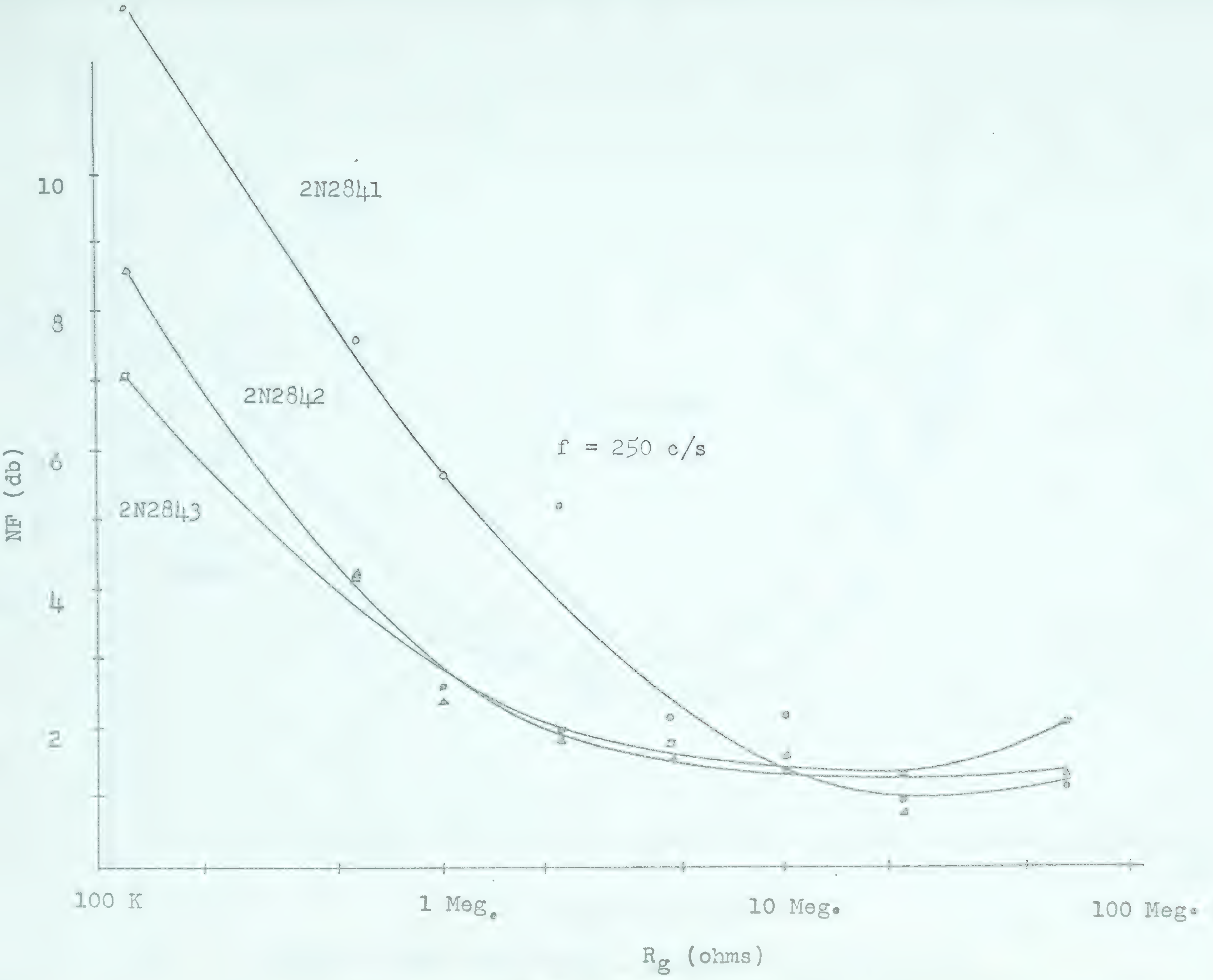
figure 3-1 Noise Measurement Setup for FET's

Using the same measurement technique as discussed in Chapter II, the results shown in graphs 3-1 and 3-2 were obtained. Although several transistors were measured, only the three FET's having the best noise characteristics are plotted. These results show that one of the 2N2842 transistors was most suitable, on the basis of noise performance, over the majority of the frequency range and over the range of source impedances called for in chapter I.

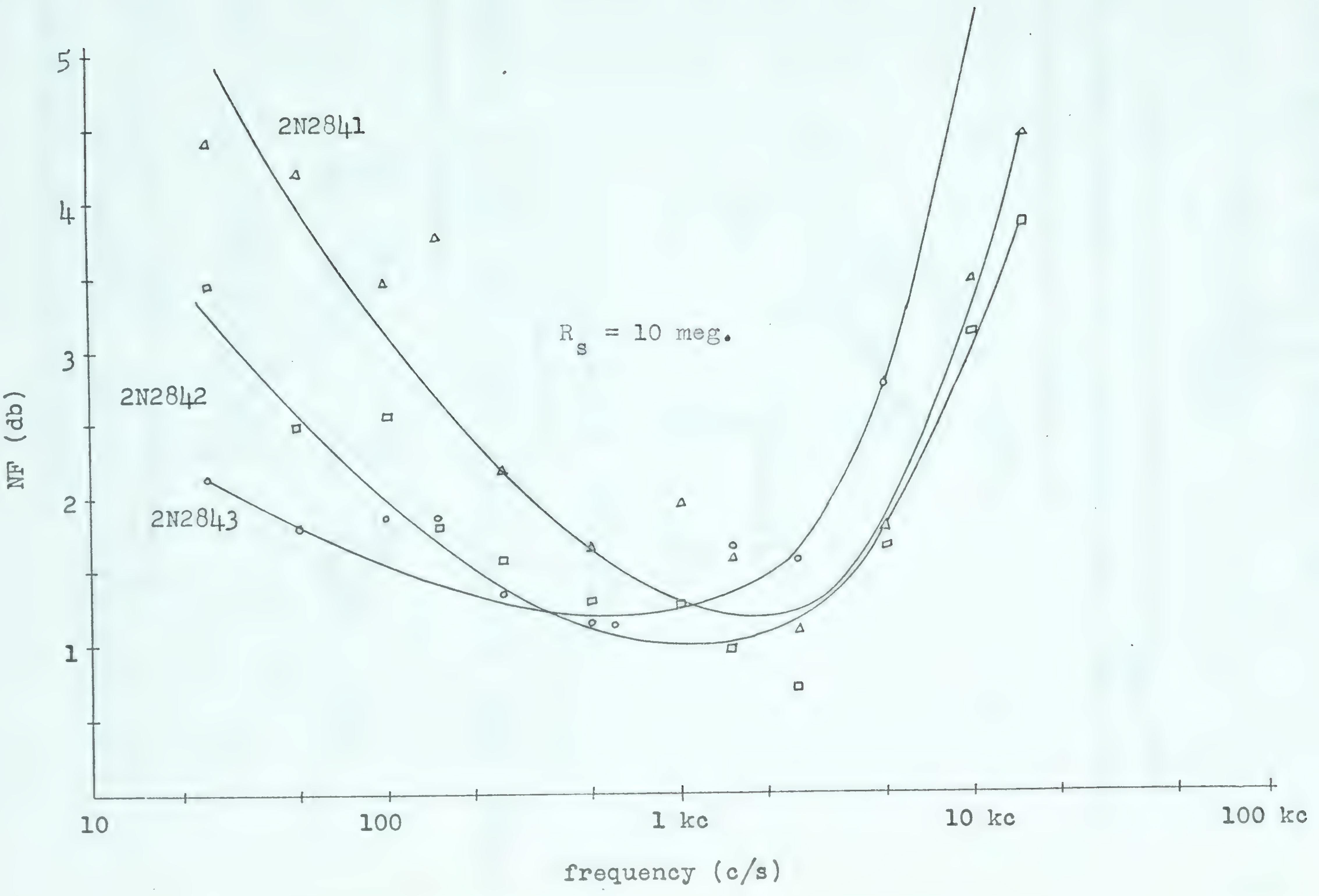
On the basis of these comparisons, the 2N2842 Siliconix field effect transistor was chosen for the input stage of the proposed amplifier.

3.2. Input Stage

In order to effectively reduce the input capacitance of the amplifier, a source follower connection was used. This reduced the gate to source capacitance C_{gs} by the factor $(1-A_{v1})$. Where A_{v1} is the voltage gain of the source



Graph 3-1 FET Noise Figure Variation with Source Impedance



Graph 3-2 FET Noise Figure Variation with Frequency

follower which is derived in Appendix I as:

$$A_{v1} = \frac{g_{fs}R_3}{1 + g_{fs}R_3}$$

Since this places a premium on a high g_{fs}, the field effect transistor was compounded with a TI415 silicon NPN transistor as shown in figure 3-2.

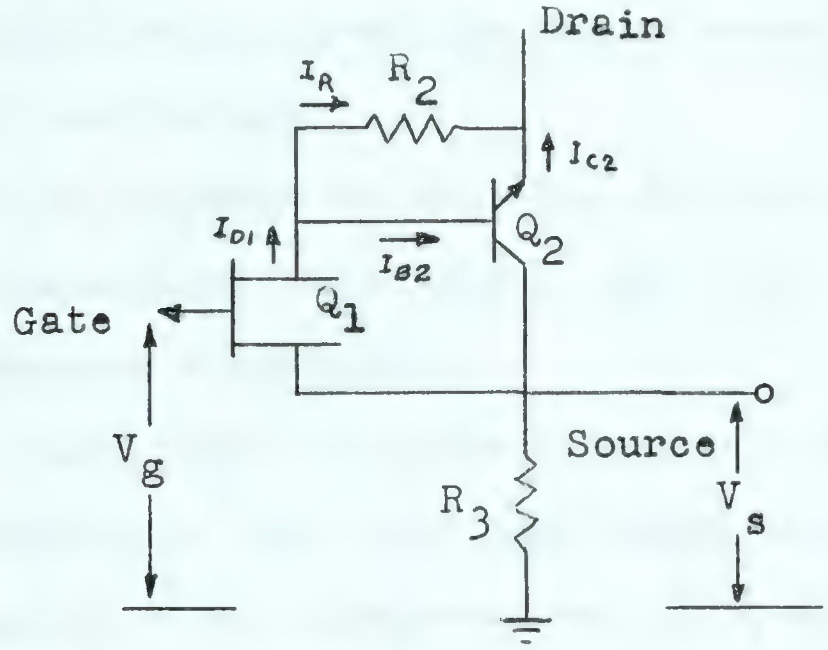


figure 3-2 FET Compound

As shown in Appendix II, this network can be considered as a single field effect transistor with common source conductance paramaters.

$$g'_{is} = g_{is} \qquad g'_{rs} = g_{rs}$$
$$g'_{fs} = g_{fs}h^{*}_{fe2} \qquad g'_{os} = h^{*}_{fe2}(g_{os} + h_{ob2})$$

where $$h^{*}_{fe2} = h_{fe2}\frac{R_2}{R_2 + h_{ib2}h_{fe2}}$$

and the subscript 2 refers to transistor Q_2

This connection, therefore, serves mainly as a transconductance multiplying network.

3.2.1. Input Stage Bias

Output current drift of a field effect transistor can be made positive, negative or zero depending upon the bias applied to the transistor(9). This is possible since the total drift is due to two effects having opposite temperature coefficients.

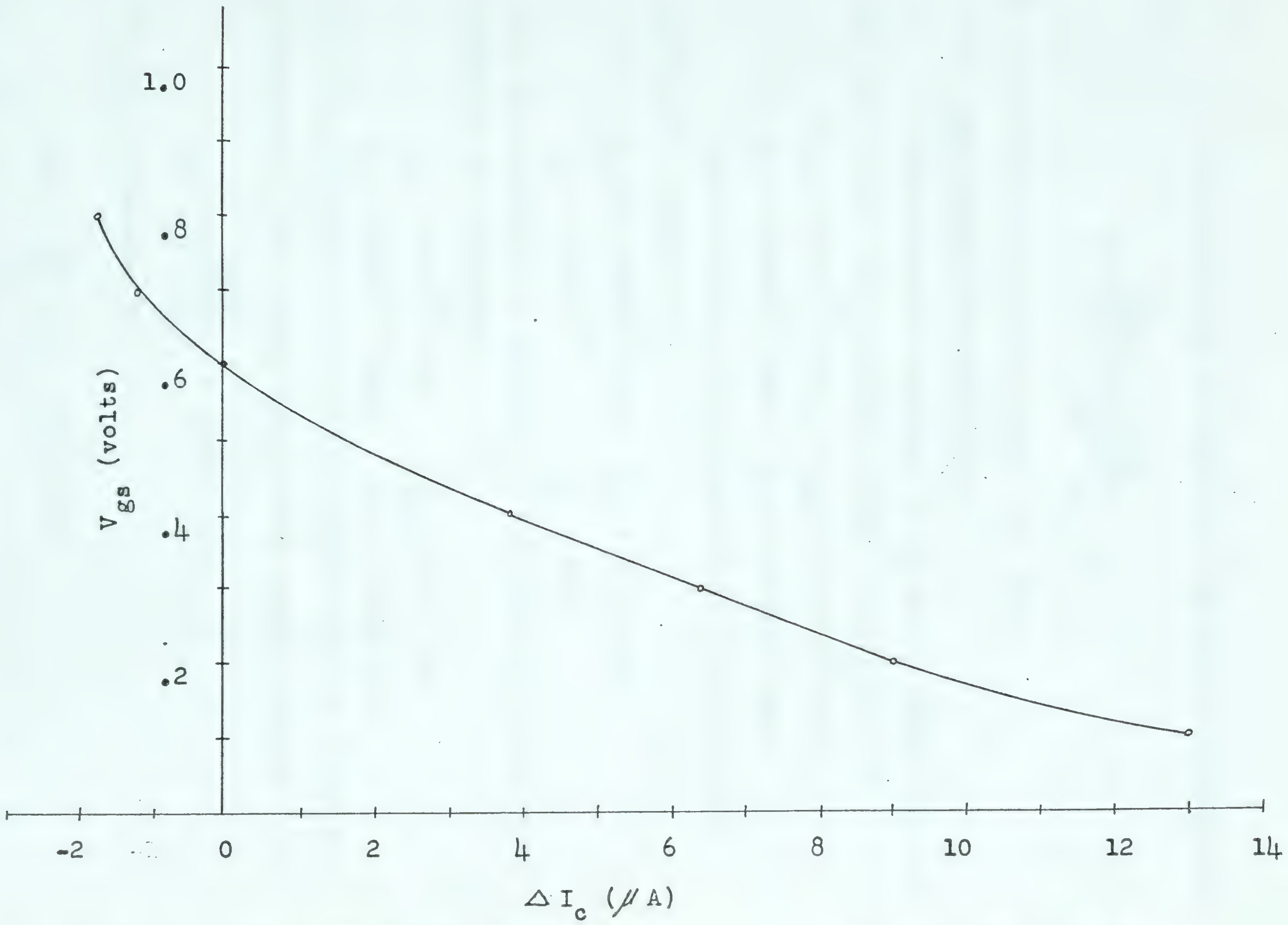
1) Normal drift of the reverse biased gate to source junction which gives the drain current a positive temperature coefficient.

2) A decrease of majority carrier mobility with increased temperature which gives the drain current a negative temperature coefficient.

A zero drift bias was considered desireable for this application so that the input stage would have the same operating point at all temperatures. This also gave a fairly small quiescent current level in the FET and allowed the use of a relatively large resistor R_2in figure 3-2. This gave the maximum possible transconductance from the compound.

In order to determine the exact bias required, drift measurements were made. The results of this test are plotted in graph 3-3, which shows that a bias of + o.6 volts would give zero drain current drift. At this bias, the drain current of the 2N2842 was found to be 45 microamps.

Since a high current gain was required of Q_2, a quiescent current of 1 ma was chosen. At this level h_{fe2} is within 10% of its maximum value. A ± 12 volt power supply was chosen, which required the use of a load resistance R_3 of 12K.



Graph 3-3 2N2842 FET Drift with a Temperature Change from 24.5°C to 57°C

The value of R_2 in figure 3-2 may also be calculated.

$$R_2 = \frac{V_{BE2}}{I_R} = \frac{V_{BE2}}{I_{D1} - I_{B2}}$$

or at the operating points chosen $R_2 = 15.1K$

3.2.2. Input Stage Characteristics

The measured paramaters of Q_1 can be taken from the input and output characteristic curves of Appendix III.

$g_{rs} = 6x10^{-12}$ mhos $\quad g_{os} = .42x10^{-6}$ mhos

$g_{is} = 20x10^{-12}$ mhos $\quad g_{fs} = 150x10^{-6}$ mhos

The paramaters of Q_2 measured at 1 ma collector current were found to be:

$h_{ob} = .05x10^{-6}$ mhos $\quad h_{ib} = 26.5$ ohms

$h_{rb} = 3.5x10^{-4}$ $\quad h_{fe} = 410$

Using the equations of Appendix II the compound conductance paramaters are therefore:

$g'_{rs} = 6x10^{-12}$ mhos $\quad g'_{os} = 10^{-4}$ mhos

$g'_{is} = 20x10^{-12}$ mhos $\quad g'_{fs} = .0348$ mhos

Several quantities can now be calculated from the equations of Appendix I. The voltage gain of the source follower is:

$$A_{v1} = \frac{g_{fs} R_3}{1 + g'_{fs} R_3} = .998$$

The output impedance is:

$$Z_{out} = \frac{1}{g'_{fs}} /\!/ R_3 = 28.5 \text{ ohms}$$

The input impedance is:

$$Z_{in} = \frac{1}{g_{is}} = 5x10^{10} \text{ ohms}$$

It is therefore obvious that the input impedance cannot be degraded very much if the specifications of Chapter I are to be met. The value of C_{gs} will be quite effectively eliminated, however, since it will be multiplied by a factor $1-A_{v1}$ or .002.

By examining the input characteristics of Appendix III, it is noticed that at the operating point chosen an input current of approximately 160 pico-amps can be expected. In Chapter I it was found that an input of less than one pico-amp was required. In order to reduce this value, current compensation was employed by connecting a 1000 megohm resistor from the gate to an adjustable portion of the source voltage as shown in figure 3-3.

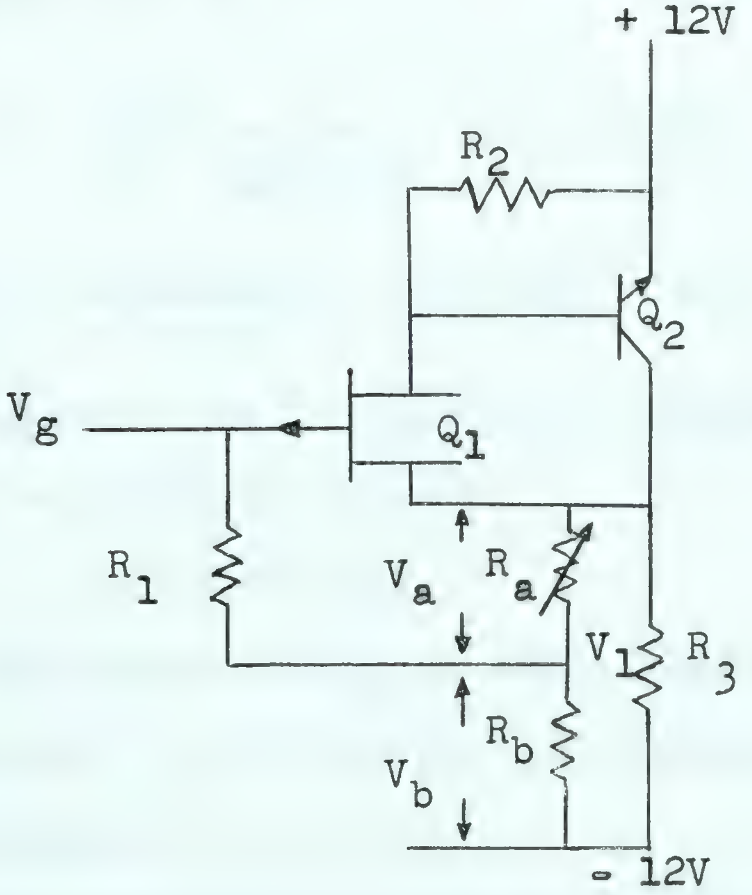


figure 3-3 Input Stage of Biological Amplifier

If the gate is at zero volts, then the required value of V_1 is:

$$V_1 = 160\text{x}10^{-12}\text{x}10^9 = .16 \text{ Volts.}$$

The ratio of R_a/R_b required is therefore

$$\frac{R_a}{R_b} = \frac{12.6-12.16}{12.16} = .0362$$

The value of R_b was chosen as 1 MΩ and R_a was made a double control, the first a 100K ohm control for coarse adjustment and the second a 3K ohm control for fine adjustment.

The effect of this current compensation resistor on the input impedance was reduced by an effective bootstrapping of the 1000 Megohm resistor.

The bootstrap gain is:

$$A = \frac{V_1}{V_g} = \frac{1}{R_a/R_b + 1} \quad A_{v1} = 0.965$$

and $$R_{eff} = \frac{1000 \text{ Meg.}}{1 - .965} = 2.85\text{x}10^{10} \text{ ohms.}$$

The input impedance will therefore be degraded to:

$$\begin{aligned} Z_{in} &= 5\text{x}10^{10} // 2.85\text{x}10^{10} \\ &= 1.85\text{x}10^{10} \text{ ohms} \end{aligned}$$

This value of Z_{in} is still acceptable by the standards of Chapter I, but it could be improved by using a larger current compensation resistor.

This stage was completed by placing a 1N66 diode in series with R_2 of figure 3-2 to compensate for the temperature drift of Q_2. The total output voltage drift of the

compound stage was then found to be 0.2 mv/ °C, which was considered satisfactory. The value of R_2 was also adjusted to 14.9 K in order to maintain a 1 ma. collector current in Q_2.

3.2.3. Noise Performance Of The Input Stage

The minimum noise that could be expected from this stage is that contributed by the field effect transistor and plotted on graphs 3-1 and 3-2. We can calculate the expected performance of the input stage by first studying the open loop circuit (fig.3-4) and then closing the loop.

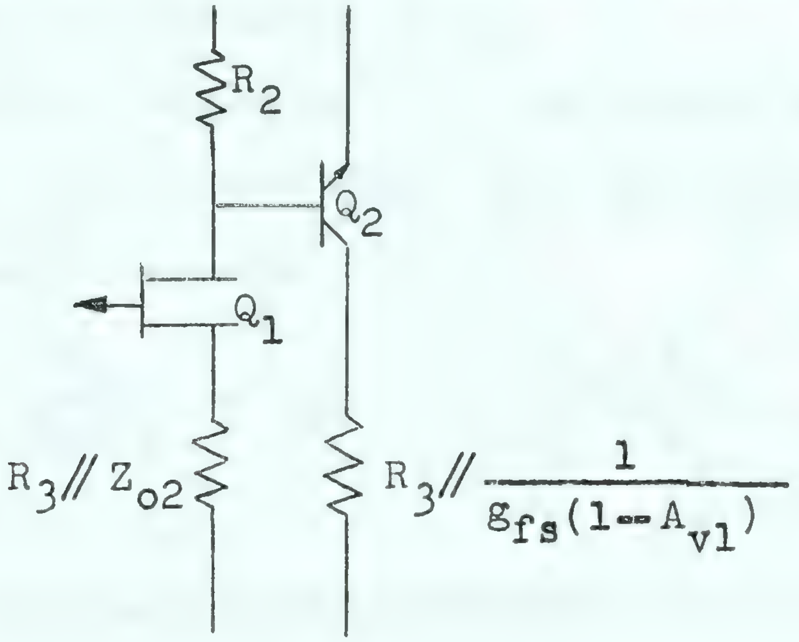


figure 3-4 Noise Equivalent Circuit of Input Stage

According to Neilson (7), the noise factor of a transistor is reduced as h_{fe} of the unit is increased. Therefore the choice of a high gain TI415 for Q_2 not only gives the maximum transconductance increase but also gives the lowest noise device.

In this same article, the source impedance R_{sopt} for the minimum noise factor of a transistor stage is calculated as being:

$$R_{sopt} = (k_2^2 + \frac{k_1}{k_3})^{\frac{1}{2}}$$

$$\text{where } k_1 \simeq r_b' + \frac{r_e}{2} \simeq \frac{h_{ib}}{2} + r_b'$$

$$k_2 = r_b' + r_e \simeq h_{ib} + r_b'$$

$$k_3 \simeq \frac{1}{2h_{fe}h_{ib}} \text{ at low frequencies}$$

Using these equations, the optimum source impedance for Q_2 at $I_c = 1$ ma is approximately 1.6K. The source impedance actually seen by Q_2 will be 14.9K in parallel with the output impedance at the drain of Q_1.

In Appendix I, equation (5), the output admittance of a common source field effect stage with an unbypassed source impedance was calculated.

$$Y_o = -g_{rs} + (\frac{g_{os}}{g_{fs}Z_g} - g_{rs}) \frac{g_{fs}/g_{is}}{1 + \frac{g_{fs}}{g_{is}}\frac{Z_E}{Z_s} + \frac{1}{g_{is}Z_s}}$$

Using this equation and paramaters given for the 2N2842 transistor, the output impedance can be calculated for a 10 megohm source impedance as being 6.8 megohms so that the source impedance seen by Q_2 of figure 3-3 will be essentially the value of R_2 or 14.9K.

Also given by Neilson is an equation relating the noise factor F, using the optimum value of R_s, to that found using a different R_s.

$$F/F_{min} = 1 + \frac{\frac{1}{2}\left(\frac{R_s}{R_{sopt}} + \frac{R_{sopt}}{R_s}\right) - 1}{1 + k}$$

$$\text{where } k = \frac{k_2 + \frac{1}{2k_3}}{R_{sopt}}$$

Therefore $F/F_{min} \simeq 1.523$

Hence this stage will have a noise factor reasonably close to its optimum value.

When n stages are cascaded the total output noise voltage can be calculated by the following equation:

$$e_n^2 = F_1 4kTR_{s1}B(A_1A_2 \cdots A_n)^2 + F_2 4kTR_{s2}B(A_2 \cdots A_n)^2 + \cdots + F_n 4kTR_{sn}BA_n^2$$

The total noise factor is:

$$F_{Total} = \frac{e_n^2}{4kTR_{s1}B(A_1A_2 \cdots A_n)^2}$$

$$= F_1 + F_2 \frac{R_{s2}}{R_{s1}A_1^2} + F_3 \frac{R_{s3}}{R_{s1}(A_1A_2)^2} + \cdots + F_n \frac{R_{sn}}{R_{s1}(A_1A_2 \cdots A_n)^2}$$

Where

R_{si} = source impedance for stage i

A_i = voltage gain of stage i

k = Boltzmans constant = 1.38×10^{-23}

T = temperature in degrees Kelvin

B = Bandwidth

The voltage gain from the gate to the drain of the FET of figure 3-4 is given by equation (6) of Appendix I.

$$A_1 = -\frac{R_2}{R_E} \frac{g_{fs}R_E}{1 + g_{fs}R_E}$$

where $R_E = R_3 /\!/ Z_{o2} = 9.9\text{k}$ and Z_{o2} is the output impedance of transistor Q_2.

$$A_1 = -0.354$$

Therefore the combined noise factor is:

$$F_T = F_1 + F_{2min} \times \frac{F_2}{F_{2min}} \quad \frac{R_{s2}}{R_{s1}A_1^{2}}$$

$$= F_1 + .018F_2 \text{ min}$$

If the feedback loop is closed, this value is not changed although the total gain of the two stages will be reduced to 0.998.

It is therefore obvious that the noise performance of the input stage wil be only slightly degraded by the addition of Q_2.

The addition of a forward biased diode in series with R_2 will not have very much effect on the first stage noise performance since it has been shown(11) that noise in a forward biased diode is equal to:

$$e_n^2 = n(4kTr_D B)$$

where r_D is the dynamic impedance of the diode and

$$n = 1 - \frac{1}{2}\,\frac{I_p}{I_p + I_{po}}$$

where I_p = current through the diode

I_{po} = reverse saturation current of the diode

Therefore $\frac{1}{2} \leqslant n \leqslant 1$ for forward bias.

Since r_D is approximately 800 ohms in this case, and n is very close to $\frac{1}{2}$, the noise voltage generated will be considerably less than that generated by R_2.

3.3 Second Stage

The need of a second stage was obviated by two

requirements:

1) Zero output voltage for zero input. The output voltage of the first stage was set at + 0.6 Volts, and therefore does not meet this requirement.

2) A gain of greater than +1 for negative capacitance feedback. The input capacitance of the first stage will still contain the capacitance from gate to drain of the 2N2842 and also stray capacitances to ground. This can be compensated for only by the use of negative capacitance feedback.

In order to obtain the above characteristics, a compound connection was used as shown in figure 3-5.

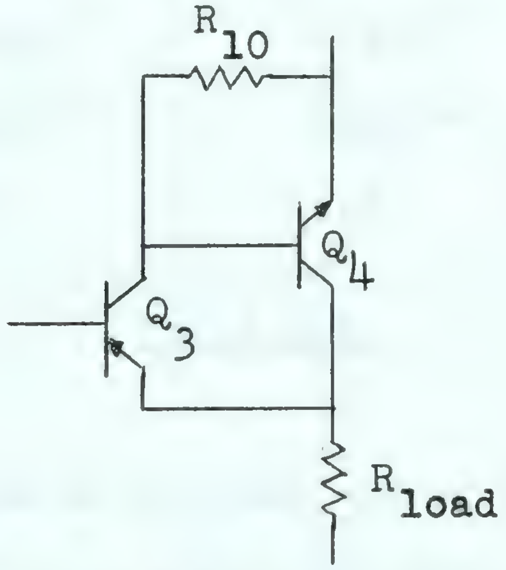


figure 3-5 Complementary Compound Connection

A 2N3251 silicon PNP transistor was used for Q_3, and a T1415 silicon NPN transistor was used for Q_4. Since a silicon transistor has a $V_{BE} \simeq 0.6$ Volts at 0.1 ma collector current, and since the output of the first stage is + 0.6 Volts, the voltage at the emitter of Q_3 will be very close to zero.

This transistor pair can also be considered as a

single transistor with h-paramaters.

$$h'_{ib} = \frac{h_{ib3}}{h_{fe4}} \qquad h'_{fe} = h_{fe3}h^{*}_{fe4}$$

$$h'_{rb} = h_{rb3} + h_{ib3}h_{ob4} \qquad h'_{ob} = h_{ob3}$$

where
$$h^{*}_{fe4} = \frac{h_{fe4}R_{10}}{h_{fe4}h_{ib4} + R_{10}}$$

The h-paramaters of Q_3 at 0.1 ma collector current and Q_4 at 1 ma collector current as well as those of the compound connection are listed in table 3-1.

	Q_3(T1415)	Q_4(2N3251)	Compound
h_{ib}	267	28	2.28
h_{ob}	$.3x10^{-7}$	$.5x10^{-7}$	$.3x10^{-7}$
h_{rb}	$2x10^{-4}$	$4x10^{-4}$	$2.1x10^{-4}$
h_{fe}	260	225	58500

Table 3-1.

The value of R_{10} was set at 8.2 K so that the collector current of Q_3 would be about 0.1 ma. This stage was also operated as an emitter follower so that a load resistor of about 12 K was required.

The voltage gain of an emitter follower is always less than one. However, for negative capacitance feedback, a voltage gain of 2 or 3 would be required. This was obtained from the compound block by placing a capacitor C_7 and an adjustable resistor R_{13} as shown in figure 3-6.

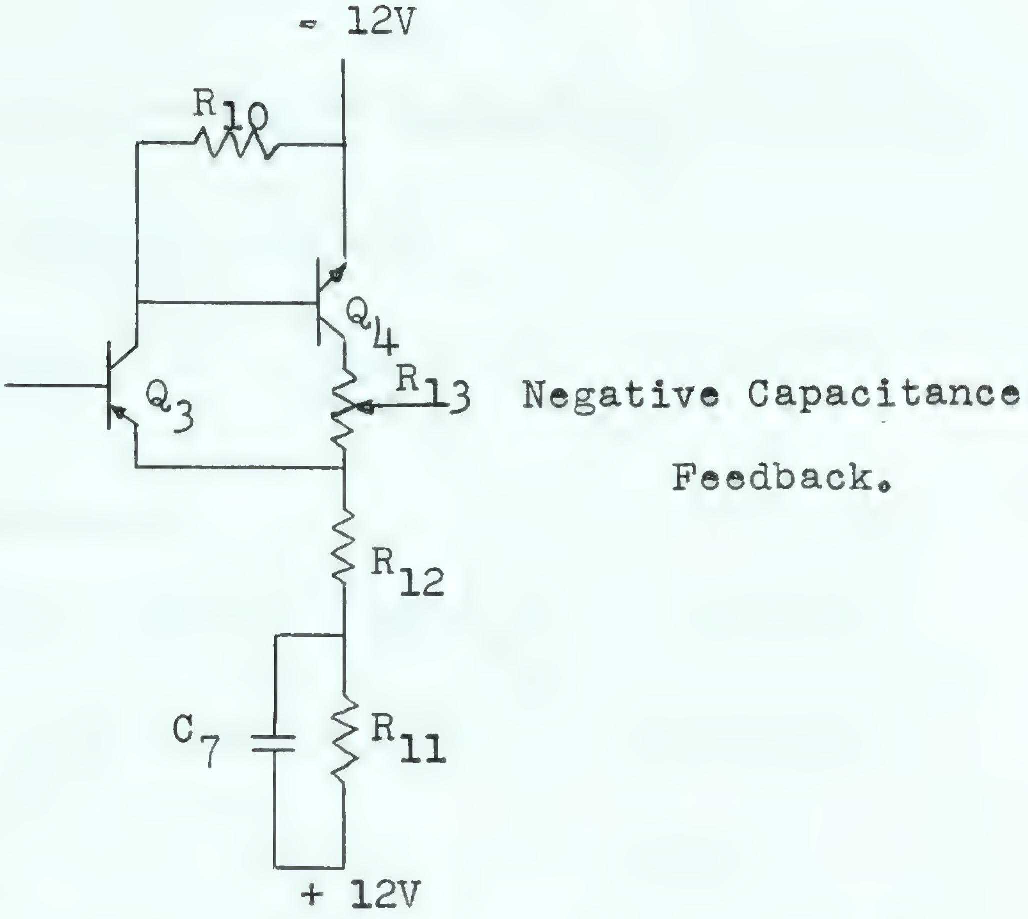


figure 3-6 Second Stage of Biological Amplifier

Where the values chosen for these components were:

R_{11} = 10K
R_{12} = 4.7K
R_{13} = 10 K
C_7 = 30μ f

Therefore I_{c4} = .815 ma. I_{c3} = .090 ma.

giving h^{*}_{fe4} = 117

Although this arrangement has a maximum gain of less than 2 at frequencies below the $R_{11} // C_7$ cut-off frequency (0.5 cps), capacitance neutralization is not required at frequencies below a few hundred cycles per second.

At high frequencies:

$$A_{v2out} \simeq 1 - \frac{h_{ib}}{R_{12}} = 1 - .49\text{x}10^{-3}$$

$$\text{max. } A_{v2feedback} \simeq 1 + \frac{R_{13}}{R_{12}} = 3.12$$

The input impedance is $Z_{in2} \simeq h'_{fe} R_{11} // \frac{1}{h_{ob}'} = 26.6$ Meg.

For dc or low frequency signals:

$$A_{v2out} \simeq 1 - \frac{h_{ib}}{R_{11}+R_{12}} = 1 - 1.55 \times 10^{-4}$$

The input impedance is:

$$Z_{in2} \simeq h'_{fe}(R_{11} + R_{12}) // \frac{1}{h_{ob}'} = 30.8 \text{ Meg.}$$

The circuit at this stage is shown in figure 3-7.

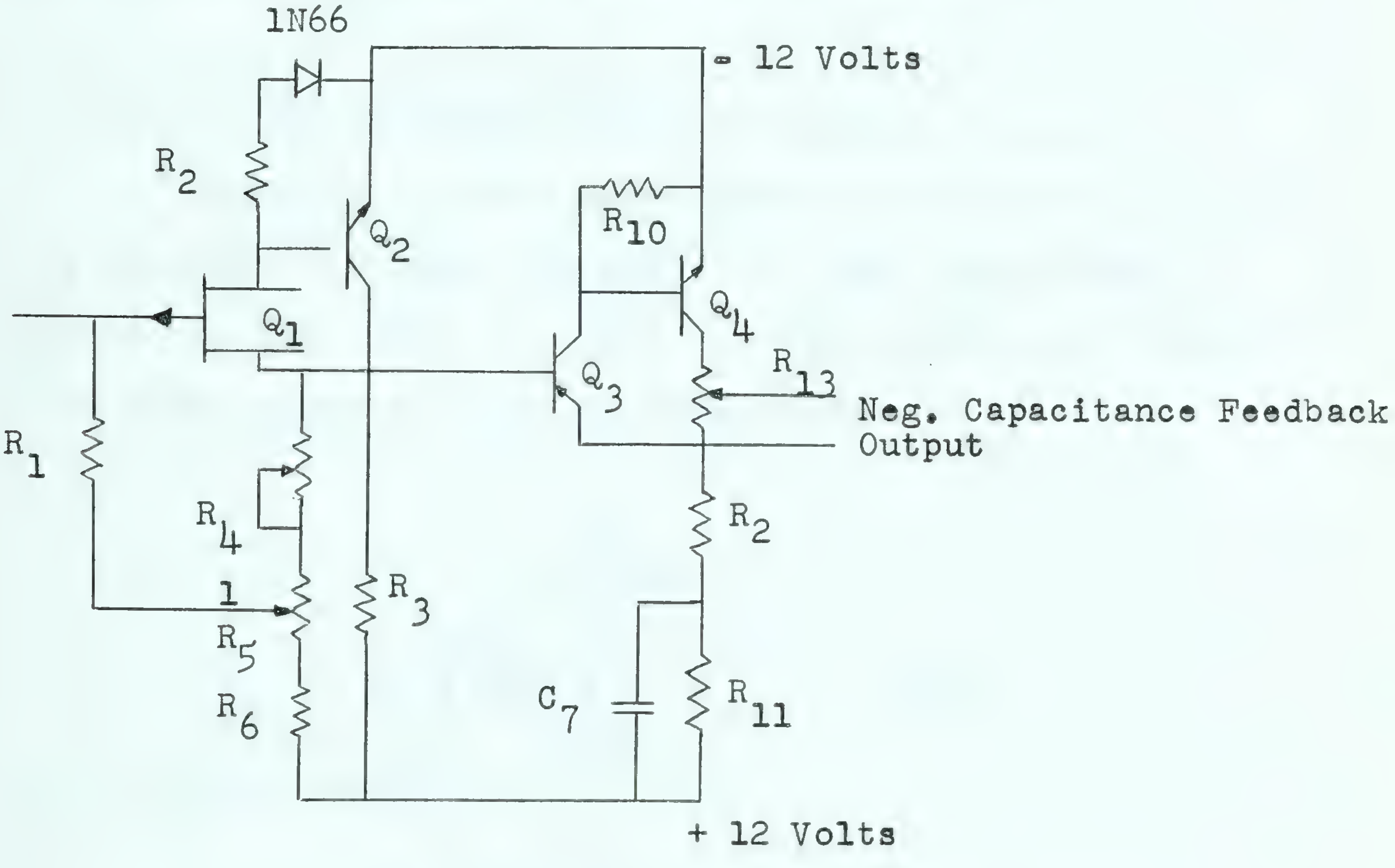


figure 3-7 Amplifier Circuit Diagram without Feedback

3.4 Negative Capacitance Feedback Loop

Noise in neutralized capacity or negative capacitance amplifiers, increases at 20 db per decade abcve a corner frequency of $\frac{1}{2\pi R_s C_{in}}$.(1)(5) The principle of negative

capacitance amplifiers is shown in figure 3.8, and shows that the feedback capacitance C_f will add to the already present C_{in}, as far as determining the upper corner frequency of the noise voltage response.

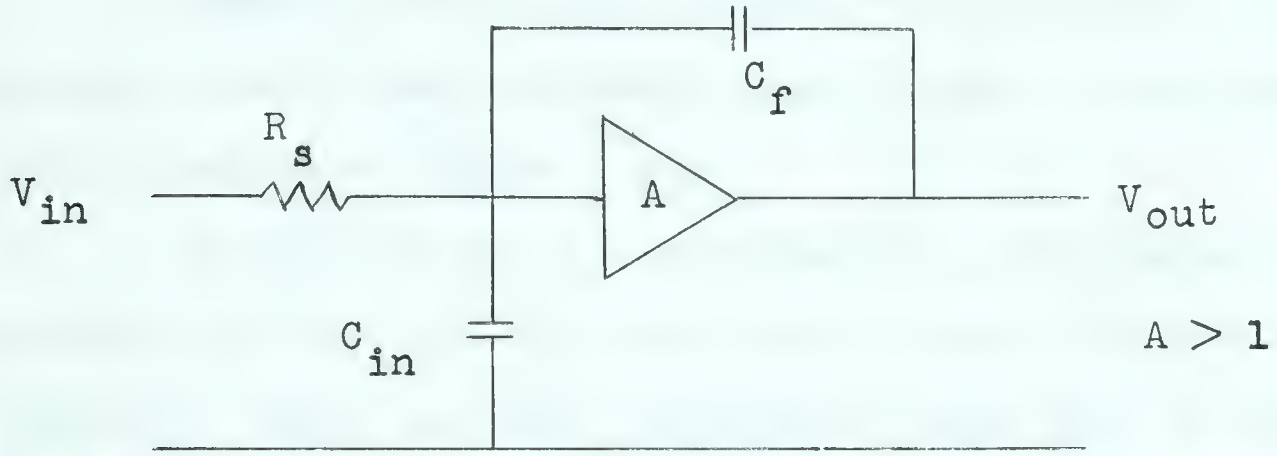


figure 3-8 Equivalent Negative Feedback Circuit

The gate to drain capacitance was used as a part of C_f in order to reduce the amount of extra capacitance added to the gate. This was done by bootstrapping the drain of the input stage as shown in figure 3-9.

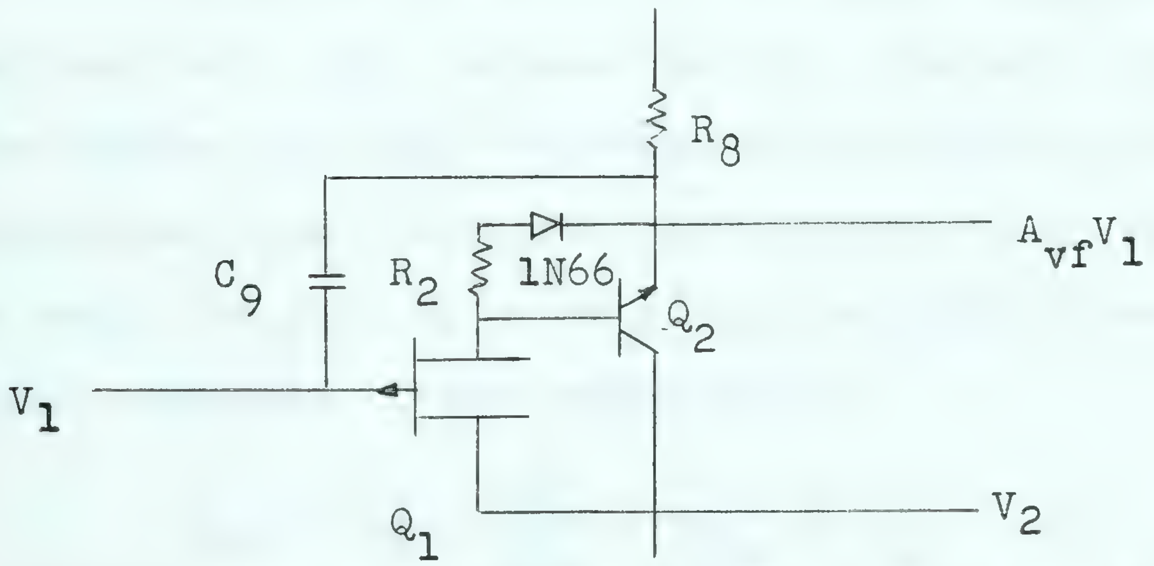


figure 3-9 Bootstrapped Drain and Feedback Capacitor

This capacitance, C_{gd}, is about 3 pf and since the total input capacitance to be compensated is expected to be about 15 pf a further capacitor C_9 of 5 pf was added. This made the maximum capacitance which could be neutralized equal

to $(A_{vf}(\max) - 1)(C_{gd} + C_9) = 17$ pf. The amount of neutralization could be increased either by increasing C_9 or $A_{vf}(\max)$.

3.5 Controls

Several adjustable controls were required at critical points. These controls are included in the complete circuit diagram of figure 3-10.

By the use of the adjustment R_7, The output voltage can be set to exactly zero volts. Since this resistance is only 100 ohms, the most the overall gain will be increased is $\Delta A_v = \frac{R_7}{R_{12}} A_{v1} \simeq 8.3 \times 10^{-3}$

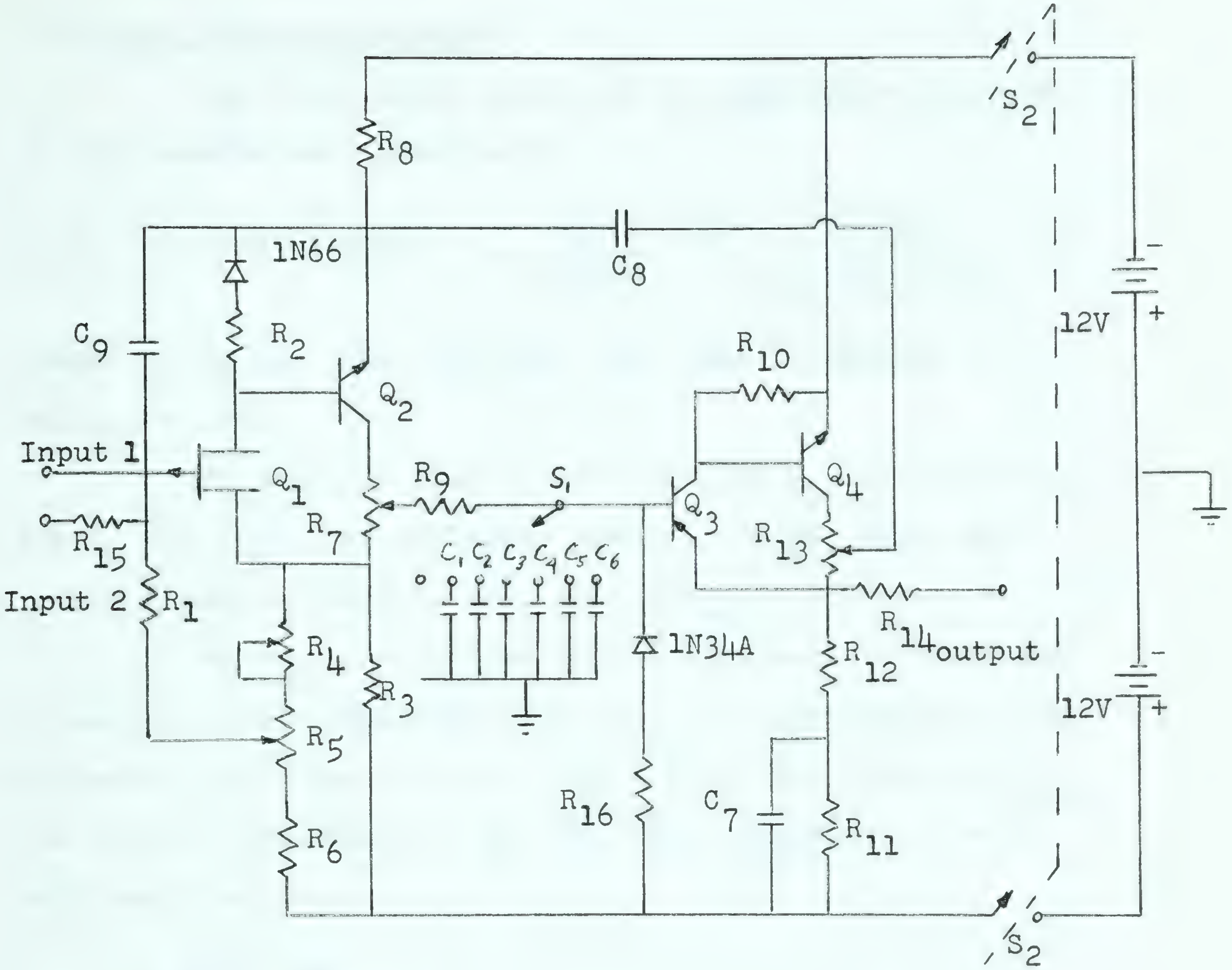
Adjustments R_4 and R_5 can be set to give zero input current and R_{13} varies the amount of negative capacitance feedback.

Switch 'S' varies the frequency response of the feedback loop. This reduces the high frequency noise but also reduces the high frequency effectiveness of the negative capacitance feedback. The addition of R_9 will reduce the amplifier gain by a factor of $1 - 8.5 \times 10^{-3}$ and sets the output impedance of the amplifier at:

$$Z_{out} \simeq h'_{ib} + \frac{R_g}{h'_{fe}} + R_{14} \simeq R_{14} = 1 \text{ K}$$

The positions 1 to 7 of the switch correspond to upper cutoff frequencies of the feedback loop of:

1) 1 Mc
2) 500kc
3) 380kc
4) 320kc
5) 180kc
6) 130kc
7) 95kc



R_1= 1K Meg.

R_2= 14.9K

R_3= 12K

R_4= 100K

R_5= 3K

R_6= 1 Meg.

R_7= 100 Ω

R_8= 1K

R_9= 10K

R_{10}= 8.2K

R_{11}= 10K

R_{12}= 4.7K

R_{13}= 10K

R_{14}= 1K

R_{15}= 10 Meg.

R_{16}= 1 Meg.

C_1= 15 pf

C_2= 25pf

C_3= 33pf

C_4= 68pf

C_5= 100pf

C_6= 150pf

C_7= 30 μf

C_8= 50 μf

C_9= 5 pf

Q_1= 2N2842

Q_2= TI415

Q_3= 2N3251

Q_4= TI415

figure 3-10 Complete Amplifier Circuit Diagram

3.6 Total Noise Performance

The total noise factor of the amplifier is given by the formula used previously.

$$F_T = F(\text{input stage}) + F_3 \frac{R_{s3}}{R_{s1}A_{v1}^2} + F_4 \frac{R_{s4}}{R_{s1}(A_{v1}A_{v2})^2}$$

Where A_{v2} is the open loop gain from base to emitter of Q_3 and $A_{v1} = .998$

The optimum source impedance for Q_3, calculated as for Q_2 but at 0.1 ma collector current, is 5K. Since the source impedance used is 10K, then $F/F_{min} \simeq 1.015$.

For Q_4, the optimum source impedance is 1.2K, and since the source impedance seen by Q_4 is approximately 8.2K, Neilson's equations give F/F min. = 1.33. The value of A_{v2} can also be calculated in an open loop configuration with only small errors.

$$A_{v2} \simeq \frac{R_{10} /\!/ Z_{in4}}{R_{12}}$$

Where $Z_{in4} \simeq h_{fe4}h_{ib4} = 7.65K$

Therefore $A_{v2} = .84$

So that the total noise figure of the amplifier is:

$$F_T = F_1 + .018F_2\,(\text{min}) + .001F_3\,(\text{min}) + .0013F_4\,(\text{min})$$

This is very close to F_1, the noise factor of the 2N2842 field effect transistor used for the input stage.

3.7 Summary of Amplifier Characteristics

$R_{in} = 1.85\text{x}10^{10}$ ohms

$A_{v(min)} = (1-2\text{x}10^{-3})(1-8.5\text{x}10^{-3})(1-4.9\text{x}10^{-4}) = 1-11\text{x}10^{-3}$

$$A_{v(max)} = (.998+8.3\text{x}10^{-3})(1-8.5\text{x}10^{-3})(1-1.55\text{x}10^{-4})$$
$$= 1-2.35\text{x}10^{-3}$$

I_{in} = adjustable to zero $\pm$ $0.1\text{x}10^{-12}$ amps.

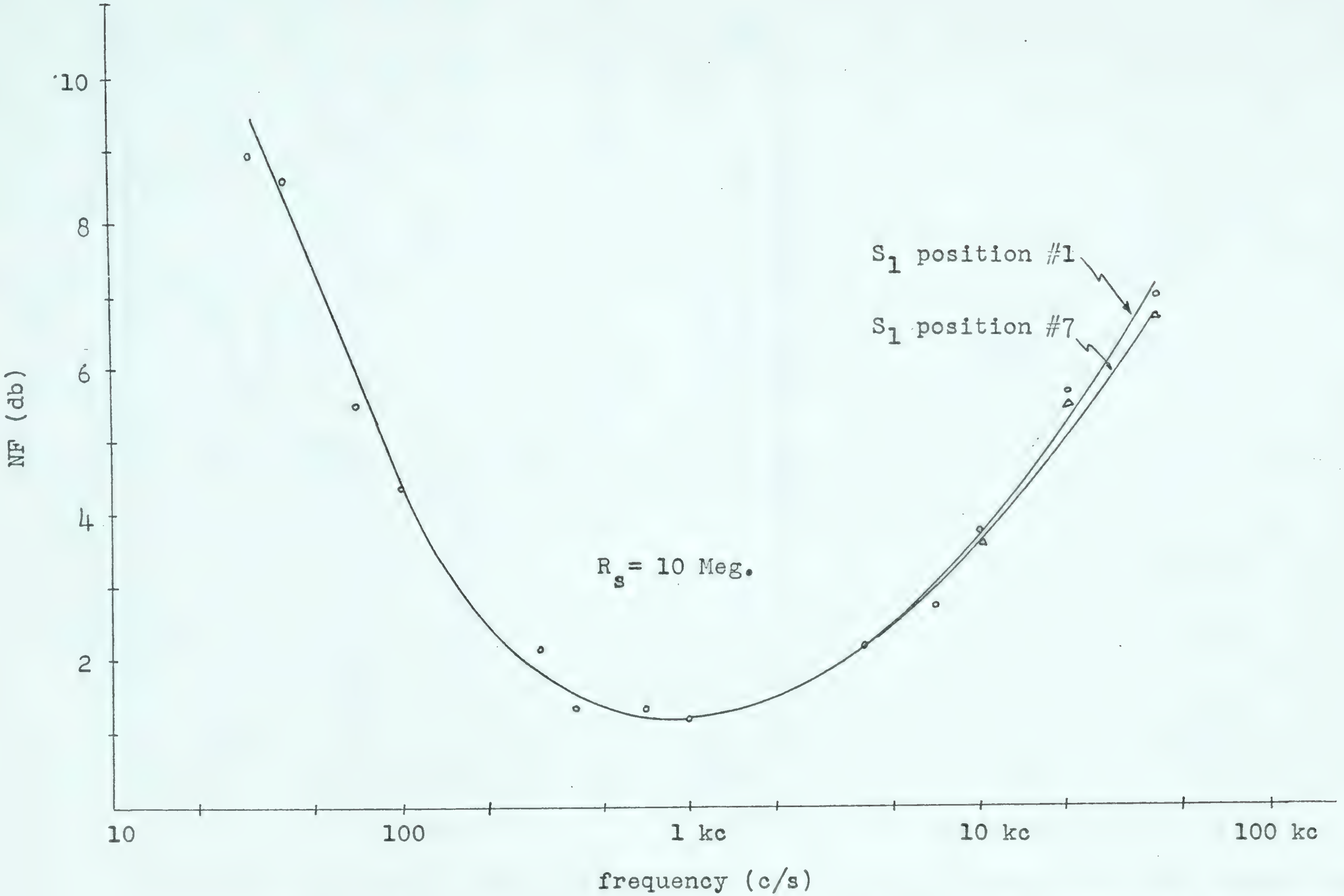
Noise Factor = approximately that of the 2N2842 field effect transistor at low frequencies and increasing at 20db/decade at high frequencies, since the F(min) of the other transistors is typically less than 1.1.

3.8 Experimental Results

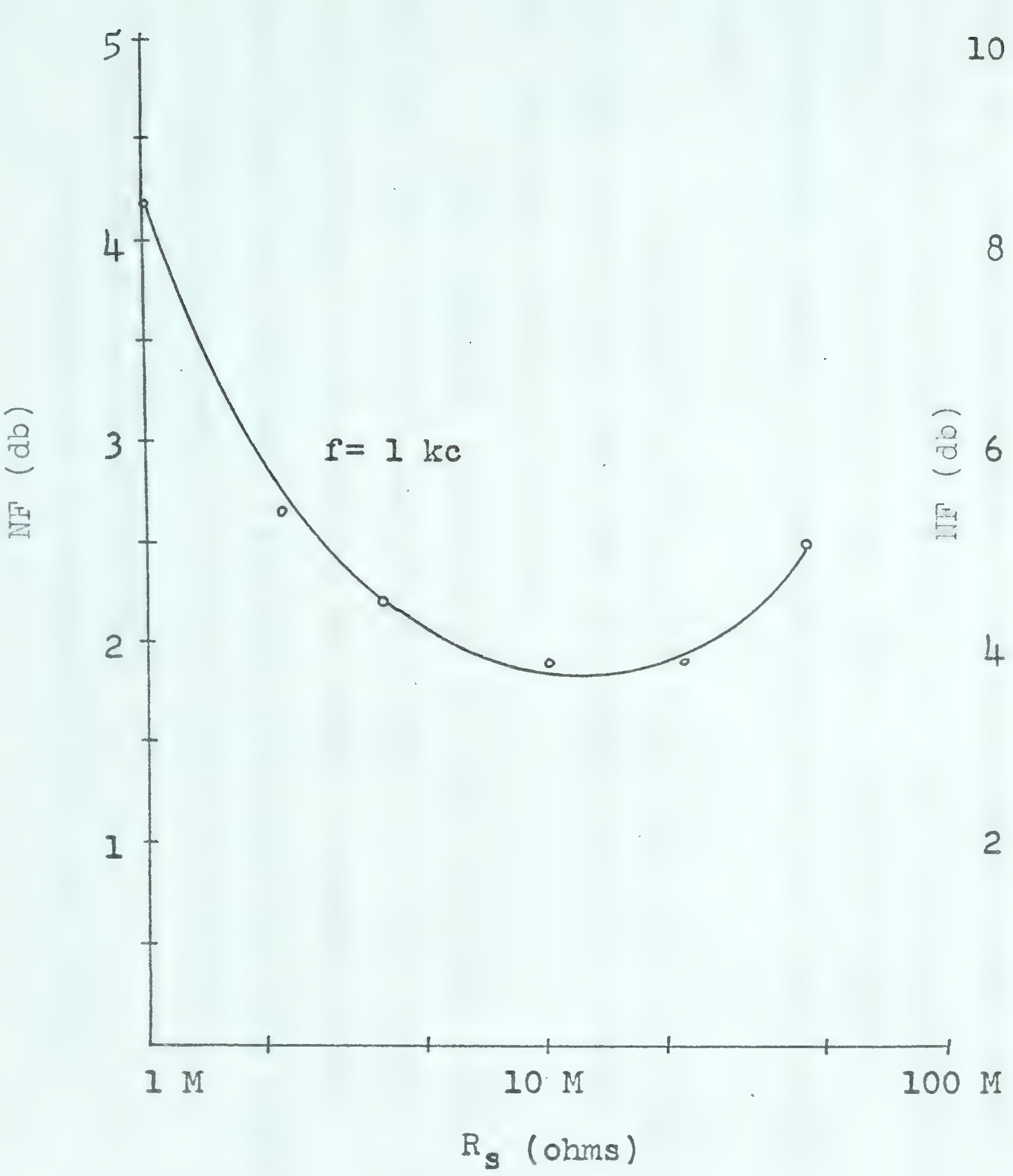
3.8.1 Static Tests

The noise performance of the amplifier was measured as a function of both frequency (graph 3-4) and source impedance(graph 3-5) by the methods discussed in Chapter II. At higher frequencies, or past the $\frac{1}{f}$ noise region, the noise figure of the amplifier was approximately equal to that of the field effect transistor, while at lower frequencies, the $\frac{1}{f}$ noise of Q_2, Q_3, and Q_4 proved to be large enough to raise the noise figure by 1 to 2 db above that of the FET. The noise figure at 10 megohms source impedance and a frequency of 1kc shown on graph 3-5 is about 1 db higher than that shown in graph 3-4 at the same frequency and source impedance. This was attributed to a higher input capacitance present during the former test, causing the high frequency noise increase to occur at a lower frequency and thus affect the noise at 1kc. This increased capacitance was present due to the necessity of having an external variable source impedance.

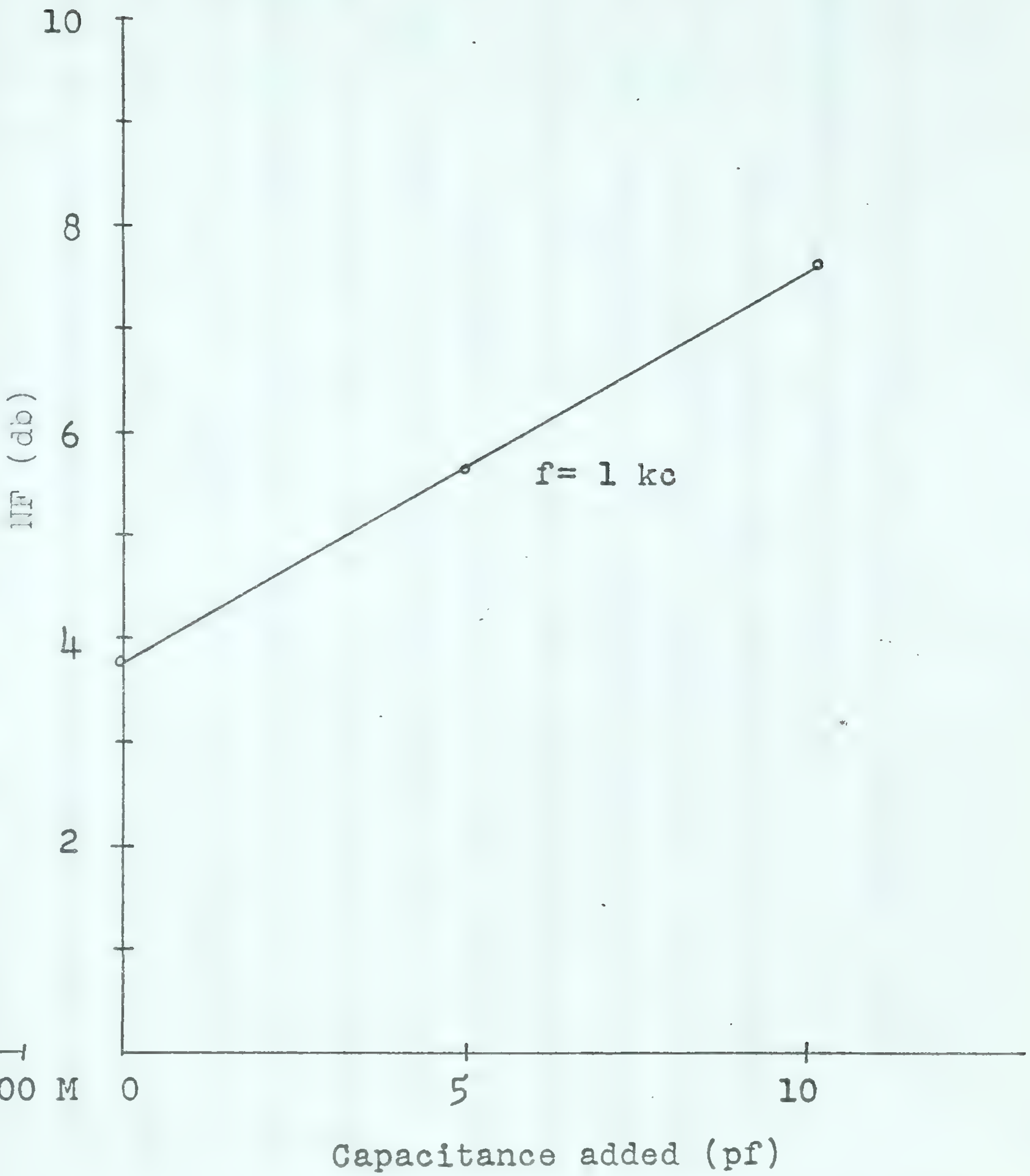
The increase in noise figure with input capacitance



Graph 3-4 Variation of Noise Figure with Frequency for Biological Amplifier



Graph 3-5 Variation of Noise Figure with Source Impedance for Biological Amplifier



Graph 3-6 Effect of Adding Input Capacitance on Noise Figure of the Biological Amplifier

was also checked at 10kc and showed a completely linear relationship. This is shown in graph 3-6.

The input resistance, measured with DC voltages, was found to be 2.1x10^{10} ohms, slightly larger than expected. The input capacitance was not measured since this is dependent only on the amount of capacitance neutralization present.

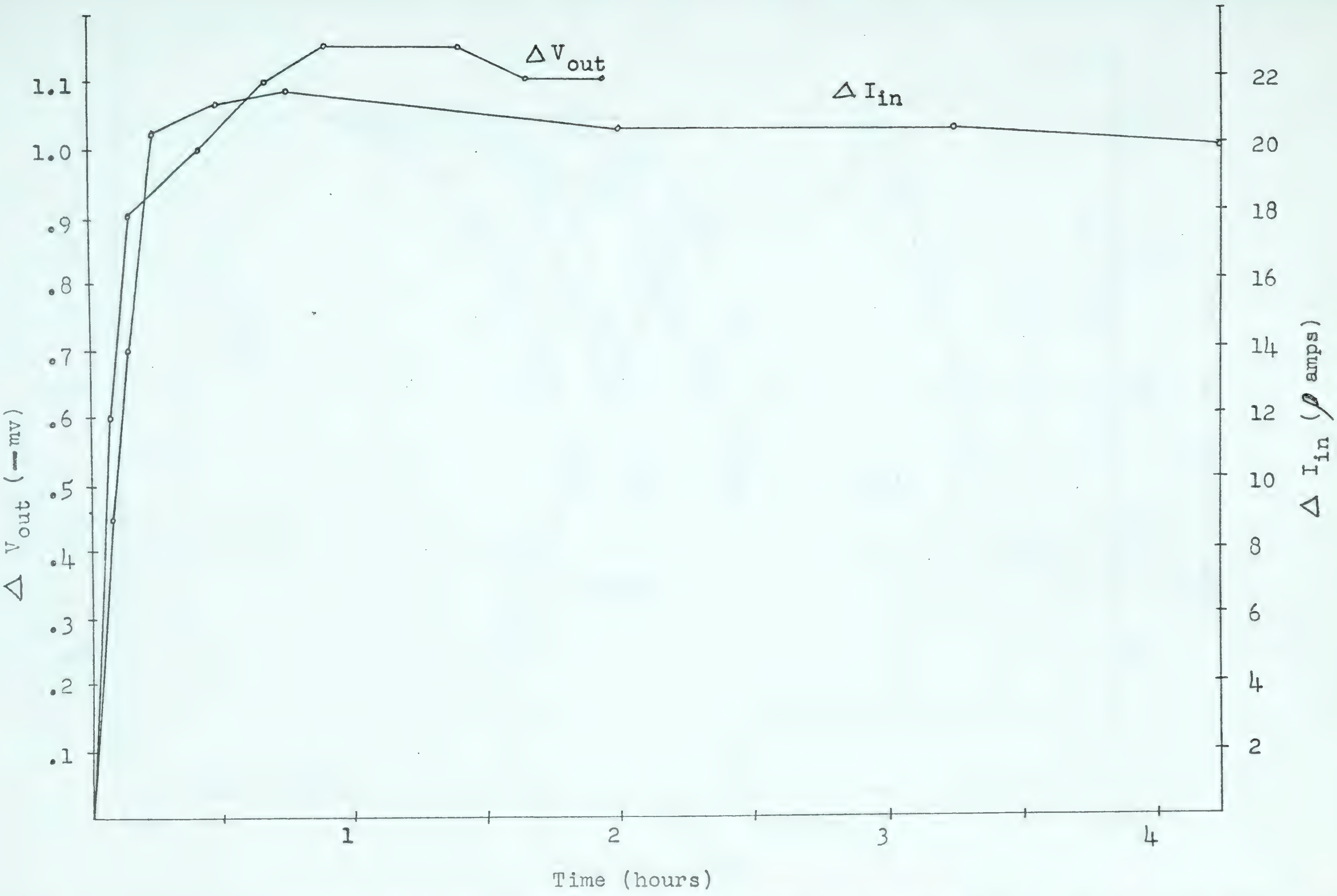
By adjustment of R_1 and R_2, the input current could be set to zero ± 0.1 pico-amps. This current drifted less than 1 pico-amp per hour, after a one hour warm-up period as shown on graph 3-7, which was attributed to a 35 mv per hour drift of the negative supply battery. Upon examination of this cell, a loose terminal was found. In order to keep this drift low, high current capacity cells should be used. (W805 Eveready instrument batteries were used for these experiments). It was also noted that an input current drift of about 5 pico-amps/hour occured if this cell was used for the positive supply.

In conjunction with these tests the output voltage drift was found to be less than 0.2 mv/hr. and .15 mv/ °C. with the input shorted to ground.

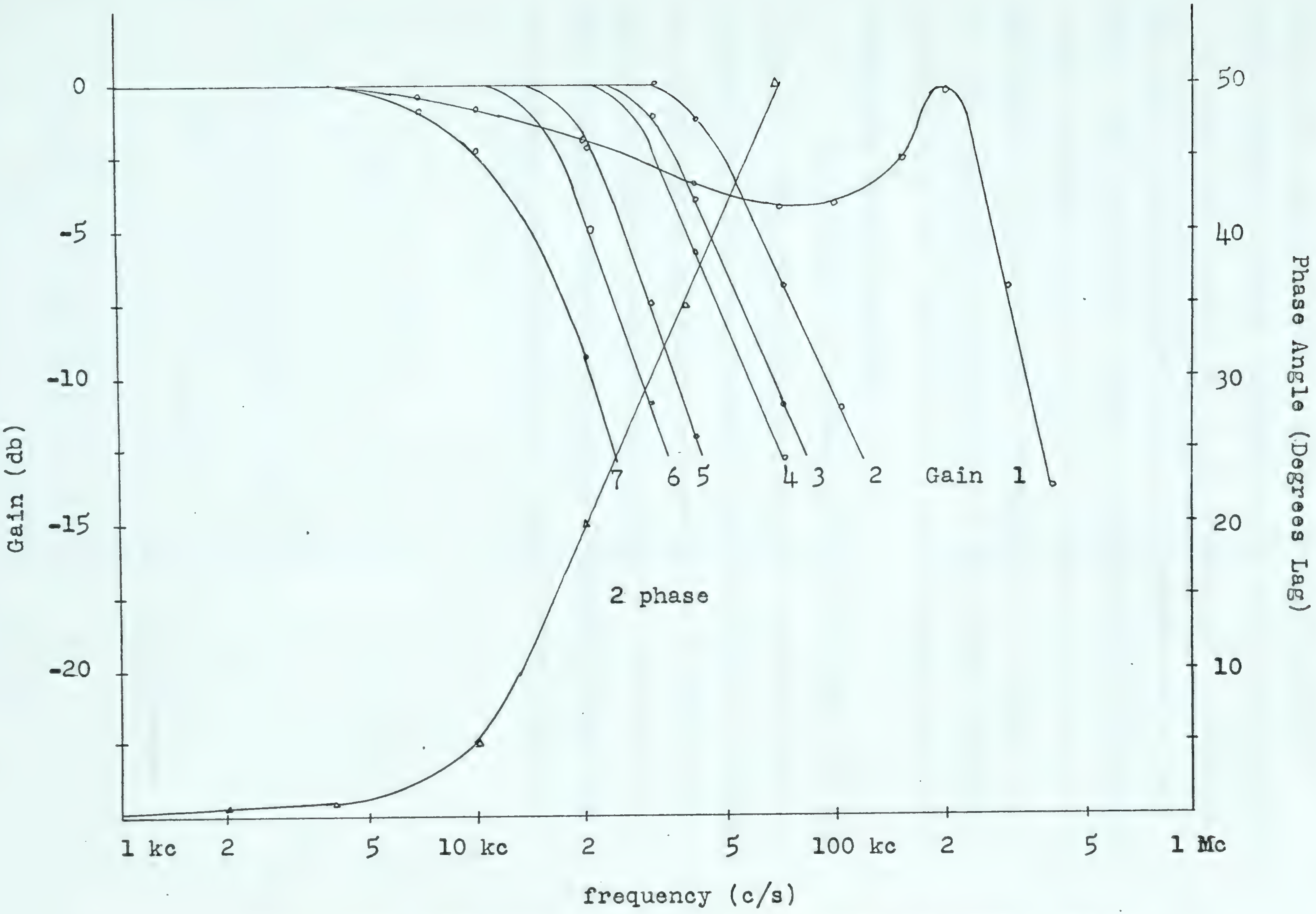
The frequency response of the amplifier was measured with unity negative capacitance gain, and a 10 megohm source impedance. These results are shown in graph 3-8 for various feedback frequency settings. Also shown on this graph is the phase angle measured under the same conditions.

3.8.2 Response To A Unit Step Input

The response of the amplifier to a 1kc, 200 mv



Graph 3-7 Output Voltage Drift and Input Current Drift as a Function of Time for Biological Amplifier



Graph 3-8 Frequency Response of FET Amplifier with a 10 Meg. Source Impedance as a Function of Switch S_1 position.

square wave applied through a 10 megohm or a 44 megohm source resistor is shown in figure 3-11. From figure 3-11(a), it is noted that a rise time of 5μ seconds can be achieved with only a small overshoot using a 10 megohm source impedance. The oscillatory response observed using a 44 megohm source impedance(figure 3-11(c)) was found to be due to stray capacitances to ground along the length of the source resistor. This was verified by placing a 1 pico-farad capacitor to ground from the junction of the two 22 megohm resistors forming the source impedance.

Decreasing the feedback cut-off frequency, as can be seen in these photographs, reduces the response time of the amplifier. This was expected since reducing the feedback cut-off frequency increases the phase shift at high frequencies causing the negative capacitance to decrease at a lower frequency. These results were obtained by measuring the frequency response with a very small source impedance.

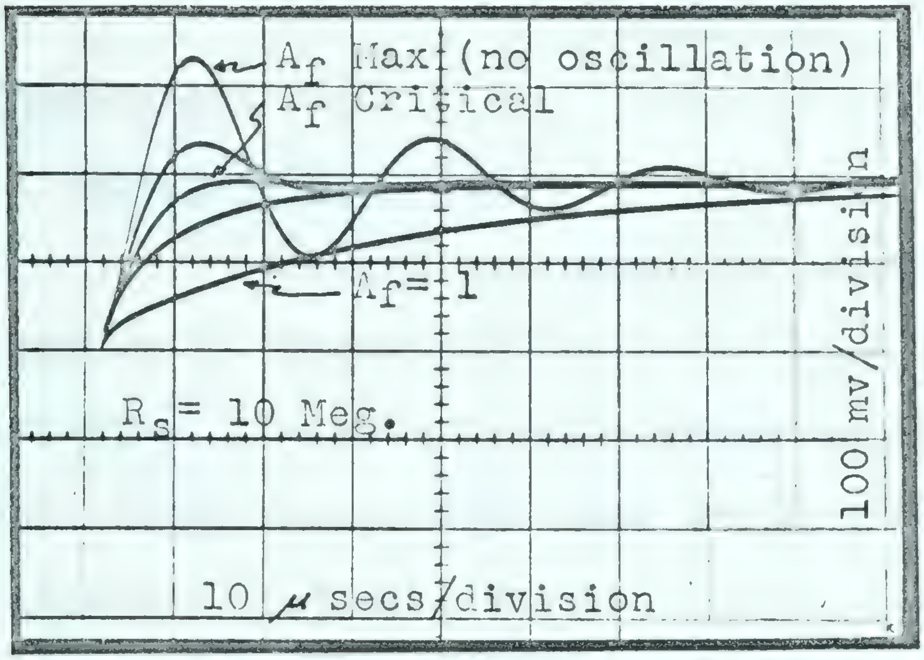


figure (a)
Variation with Negative
Capacitance Feedback.

S_1 position #2

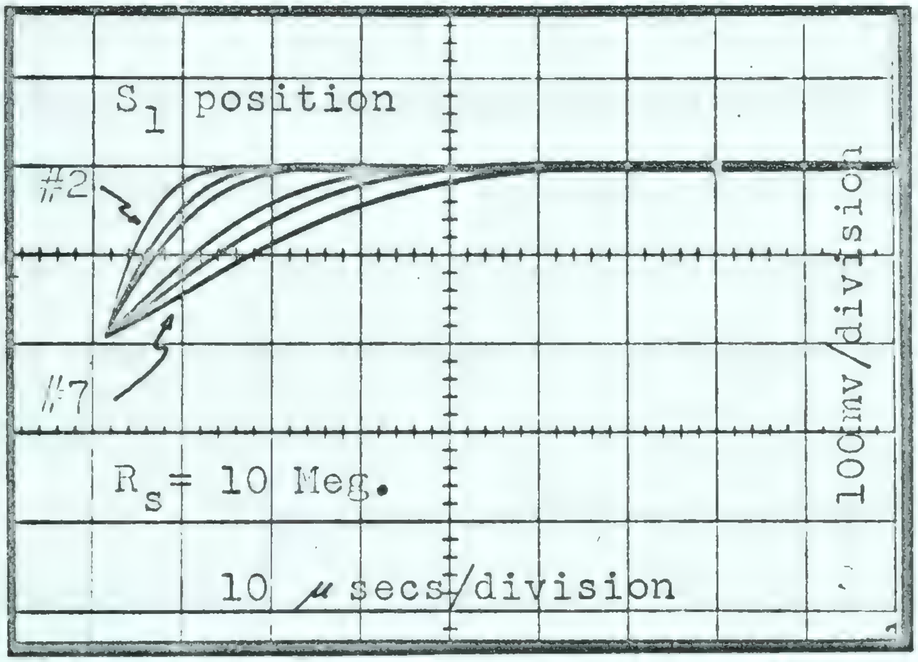


figure (b)
Critical Damped Response
Variation with Feedback
Cutoff Frequency

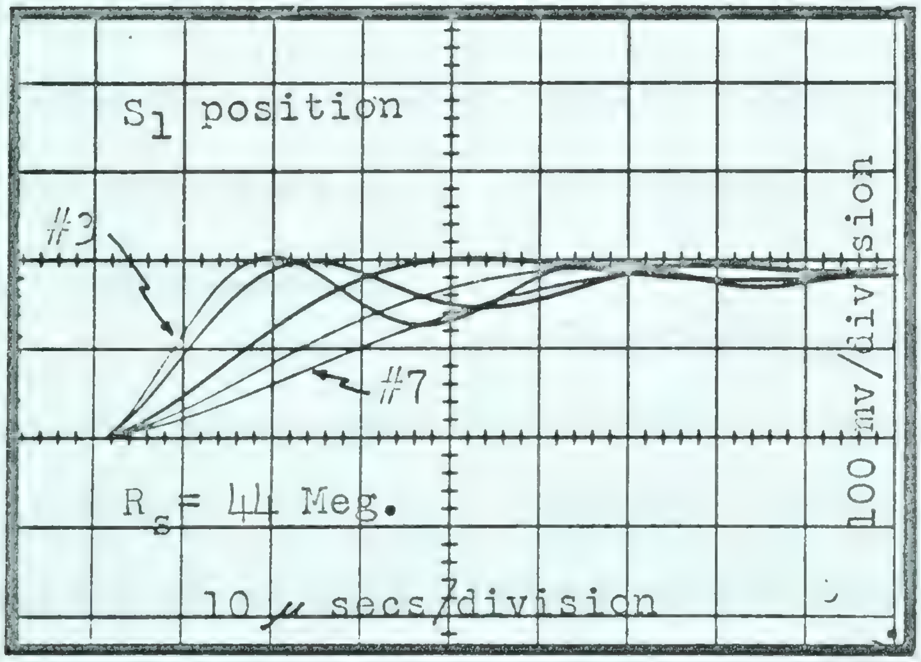


figure (c)
Critical Damped Response
Variation with Feedback
Cutoff Frequency

figure 3-11 Amplifier Response to Square Wave Input

Chapter IV

Conclusions

4.1 Circuit Operation

Although the amplifier meets the requirements of chapter I, improvement could be made in some of the characteristics. The main trouble point is the input current drift with temperature. Since the field effect transistor input is basically that of a reverse biased diode, it is impossible, with this device, to keep the input current from changing less than 50 to 100 pico-amps with a 10°C. temperature change. One method of compensating for this current, is to use a reverse biased diode in the current compensation network. This, however, has a detrimental effect on the noise performance of the amplifier at high frequencies due to the added capacitance which is present in a diode.

The input resistance of $2x10^{10}$ ohms also meets the requirements of chapter I, but it would be preferable to raise this value by one or two orders of magnitude. This is much larger than the inherent input resistance of a field effect transistor. The level could be increased by the use of a circuit employing D.C. bootstrapping of source to drain.

4.2 Future Trends

There is now available a fairly similar device in the insulated gate field effect transistor commonly called a MOS FET. The input impedance of this device is limited mainly by surface leakage of the transistor's encapsulation material, and can be as high as 10^{17} ohms. In conjunction with this high input impedance, the input current is low

enough that current compensation would not be required.

At the present time, the only failing of these devices is a very high, low frequency noise figure. This noise is of an f^{-n} nature, where n is typically between 1 and 2, and may extend into the megacycle region.(12) Two typical devices available at this time, a 1005 General Micro-Electronics unit and an FI100 Fairchild unit, were tested with a 10 megohm source impedance and gave a noise performance as shown in graph 4-1.

The more recently manufactured Fairchild unit shows a considerable improvement over the 1005 transistor. If this trend to improved low frequency noise figures continues, the MOS FET would be ideally suited to measuring action potentials.

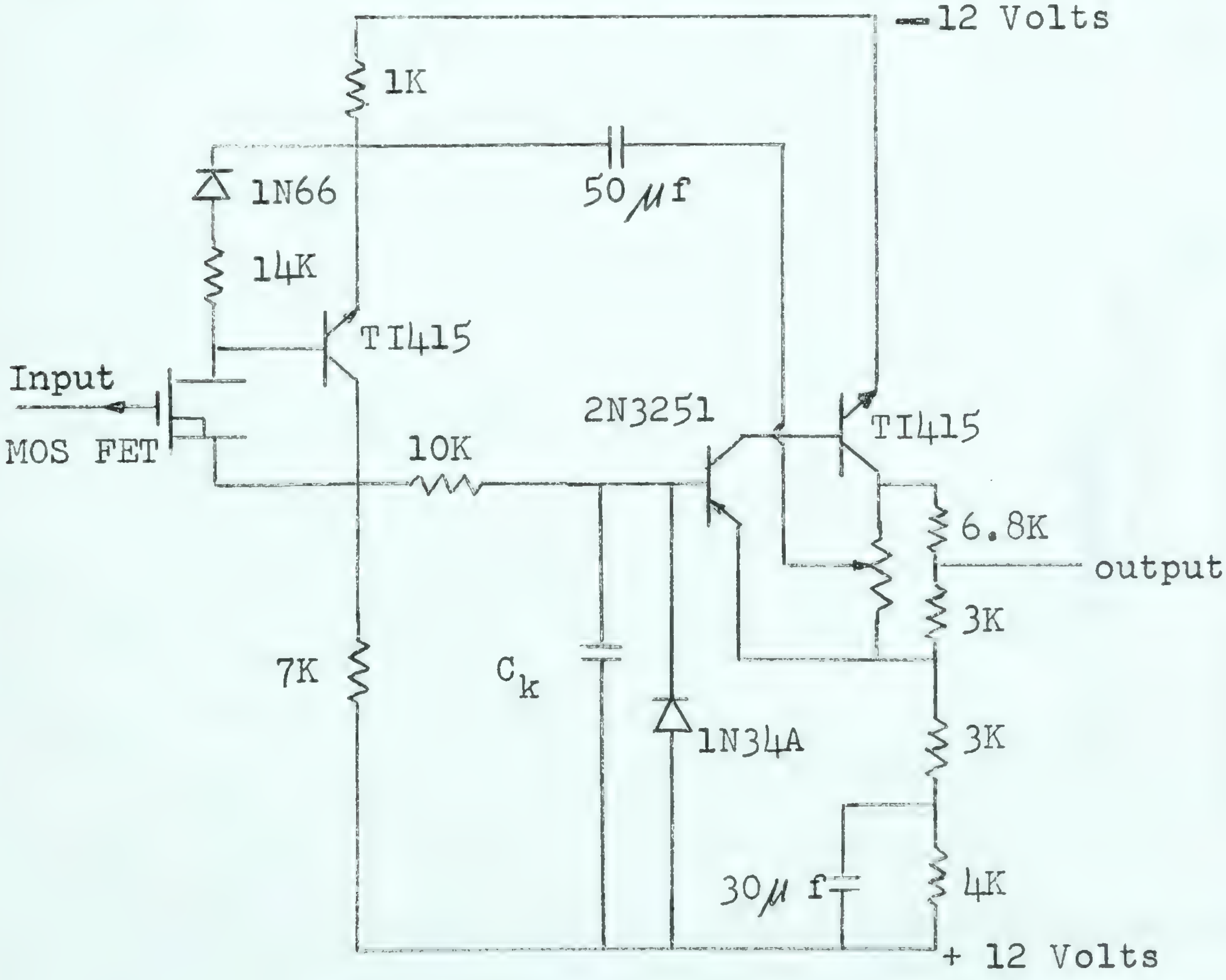
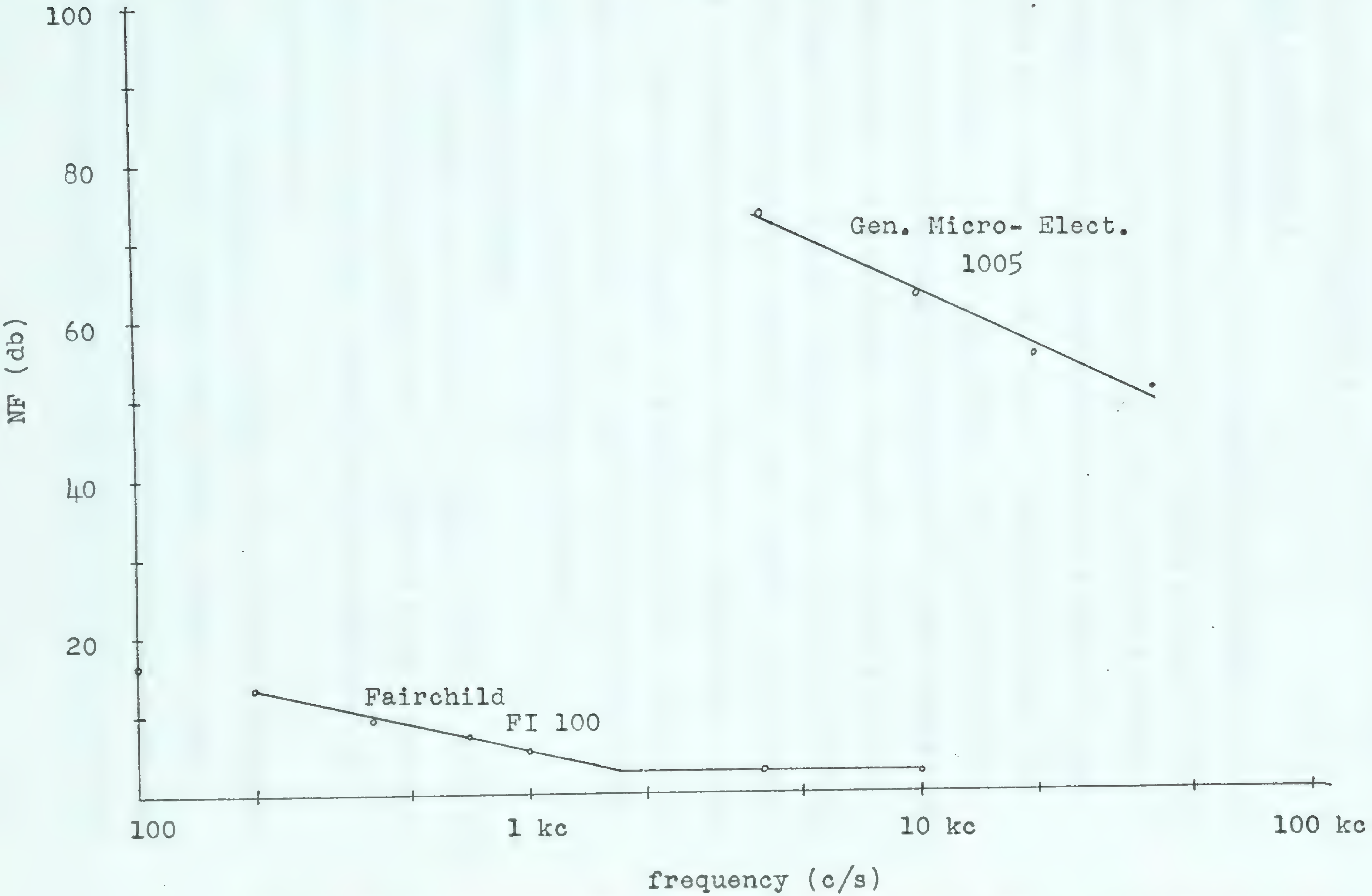


figure 4-1 Proposed MOS FET Circuit Diagram



Graph 4-1 Noise Figure vs Frequency of MOS FET's at 50 amps Drain Current

A proposed circuit similar to that designed previously but using an enhancement type MOS FET and having a gain of 2 is given in figure 4-1.

4.3 Space Requirements

One advantage of the transistorized amplifiers is the ability to build them into a very small package in order to make multiple readings along a nerve. With the methods known today, it would be feasible to build either of these amplifiers in a space of only one or two cubic inches (excluding controls). Recent experiments with growing single crystal silicon on insulating substrate(13) also brings about the possibility of a completely integrated circuit of extremely small size. Already perfected are methods of forming NPN silicon and p-channel FET's on one chip(4), as well as methods of forming complementary compound transistors on one chip(15). Therefore it would be possible to form the active components on, at the most, two chips and to form the passive components on a third insulated substrate.

4.4 Biological Performance

The amplifier was used to measure action potentials present in a milenated nerve fibre connected to the sartorious muscle of a frog. The set-up for this experiment is shown in figure 4-2.

The amplifier was adjusted to a critically damped condition by feeding a square wave pulse through a very small capacitor (< 1 pf) into the amplifier input. This gave an impulse signal into the amplifier which was then used to

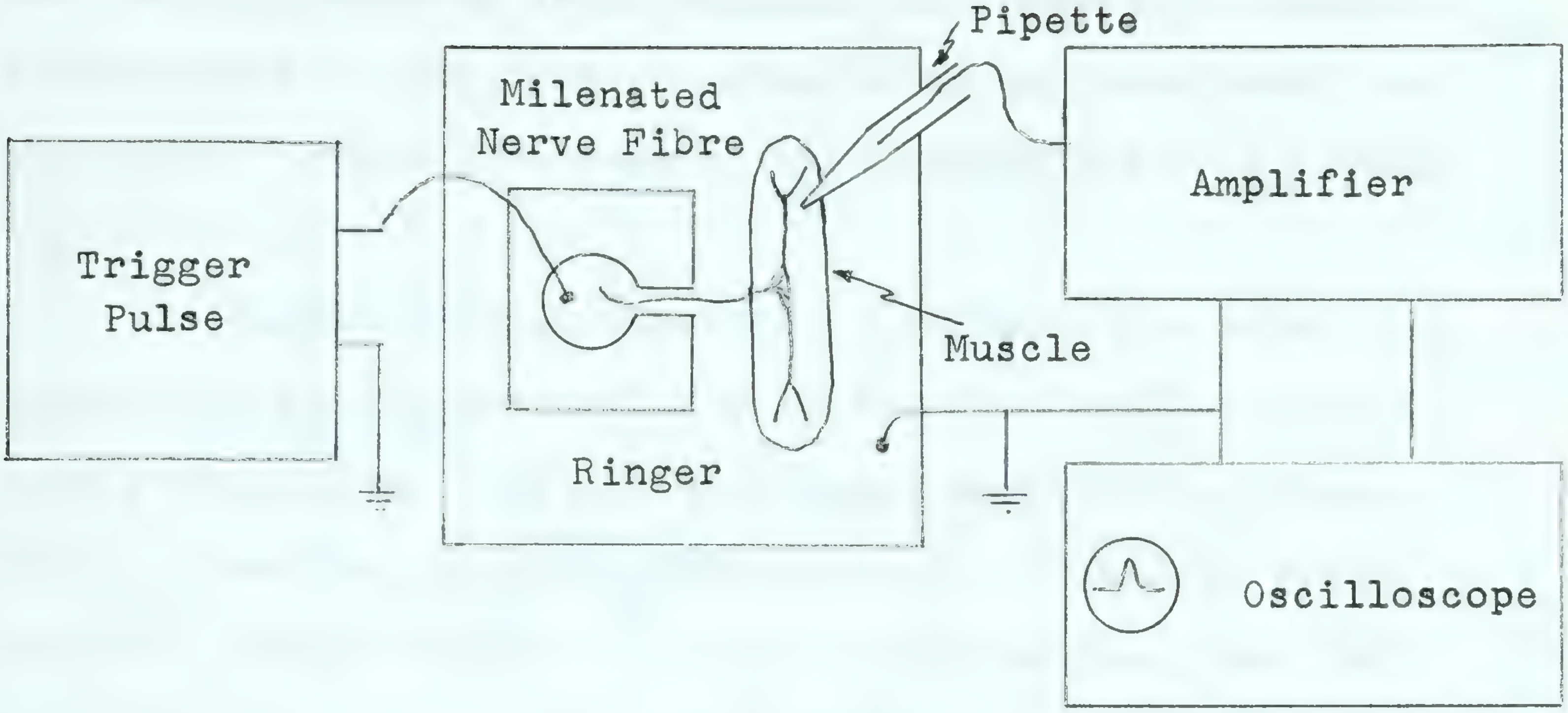


figure 4-2 Biological Test Set-up

adjust the negative capacitance feedback until only a slight ringing was present at the amplifier output. The square wave used was generated by the circuit of figure 4-3, which could be incorporated into the completed amplifier, if desired.

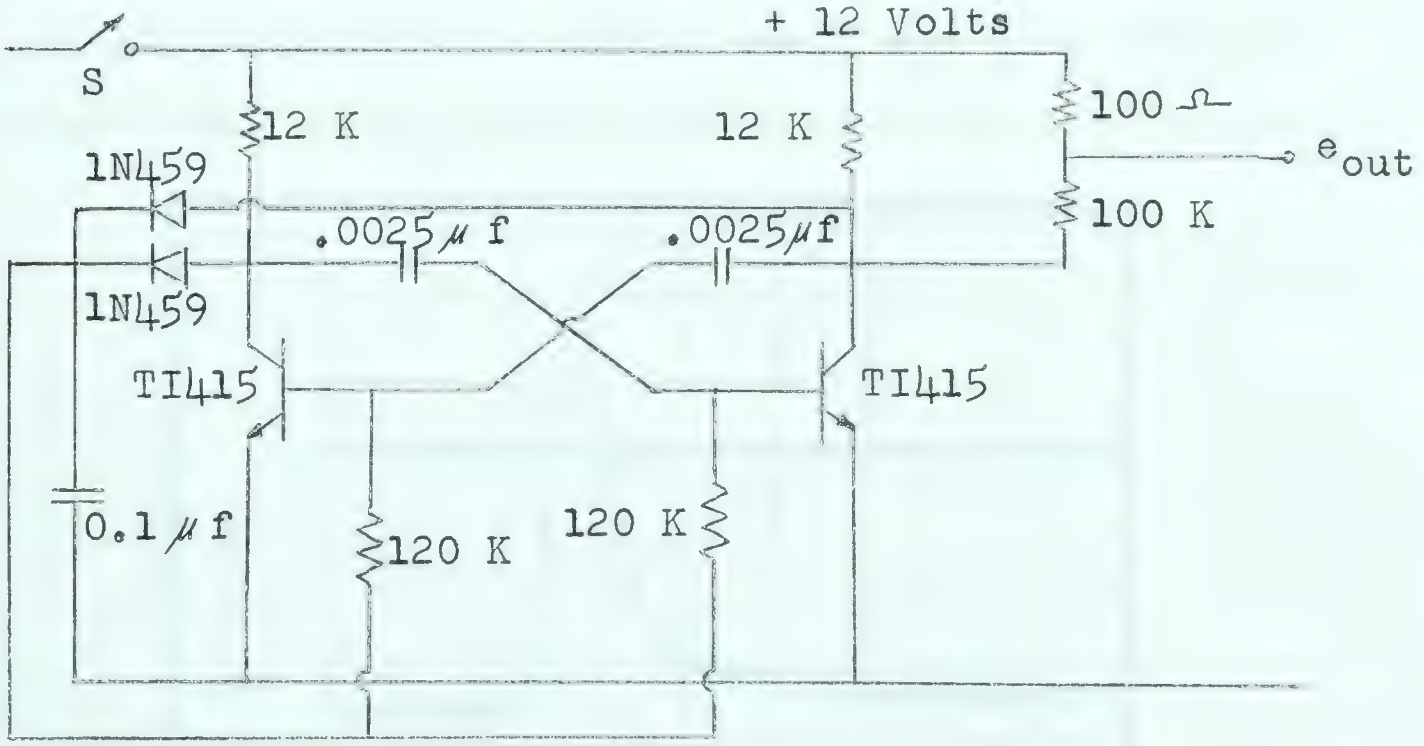


figure 4-3 Astable Multivibrator Circuit

Before performing the experiment, the tip resistance

was roughly measured as 50 megohms. The actual tip resistance present at the time of measurement may have been less than this, however, because of the possibility of a broken tip.

After several attempts, a potential as shown in figure 4-4 was observed. The wave form was typical with a rest potential of − 55 mv and a pulse amplitude of 80 mv, with a rise time of about 200 μ seconds and a fall time of about 1200 μ seconds. It must be pointed out that this was not a severe test for the amplifier, but it did serve as a check on major performance drawbacks. For a complete evaluation of the amplifier, a reasonable amount of varied physiological use would be required. The incorporation of the test circuit of figure 4-3, would appear to be a very useful addition. The addition of the 10 megohm resistance (R_{15} of figure 3-10) to a second input was also found to be quite useful for determining the resistance of the tip.

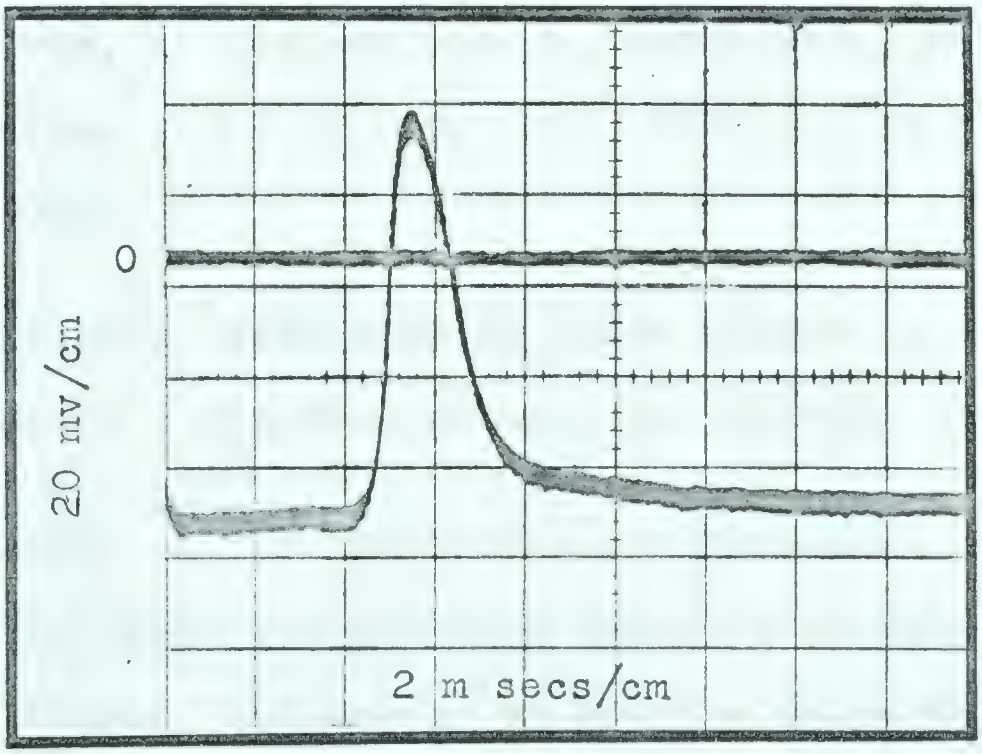


figure 4-4 Frog Action Potential

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Appendix I

FET Paramaters

An FET can be described by common source y-paramaters as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} g_{is} & g_{rs} \\ g_{fs} & g_{os} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

The equivalent circuit using these paramaters is:

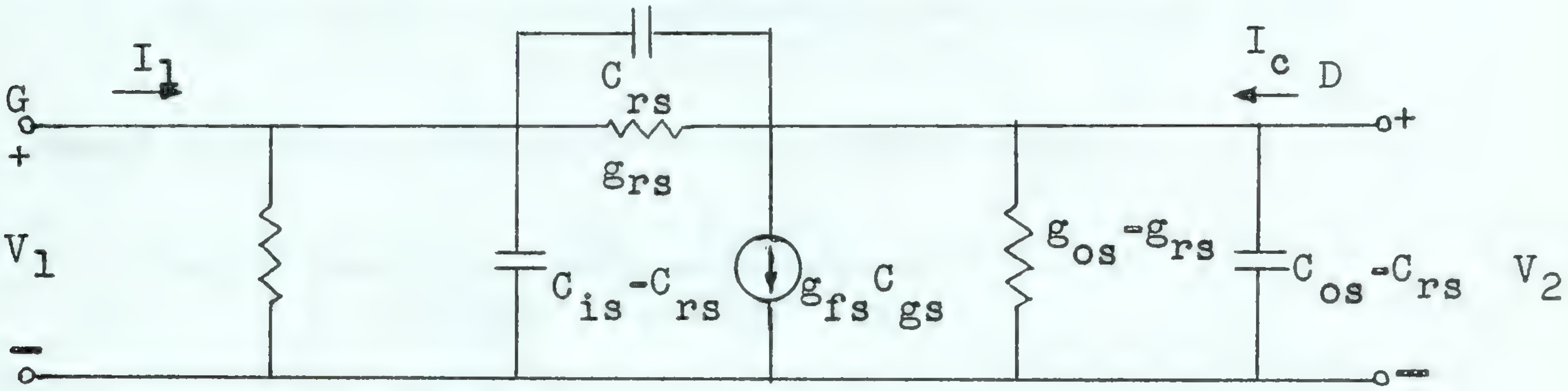


figure I-1 FET Equivalent Circuit

These can be converted to h-paramaters to give:

$$\begin{bmatrix} h_{ie} & h_{re} \\ h_{fe} & h_{oe} \end{bmatrix} = \frac{1}{g_{is}} \begin{bmatrix} 1 & -g_{rs} \\ g_{fs} & g_{is}g_{os} - g_{fs}g_{rs} \end{bmatrix}$$

These can be converted to common base paramaters by means of well known paramaters conversion equations (10)

$$h_{ib} = \frac{1}{g_{is} + g_{rs} + g_{fs} + g_{os}} \simeq \frac{1}{g_{fs}}$$

$$h_{rb} = \frac{g_{os} + g_{rs}}{g_{is} + g_{rs} + g_{fs} + g_{os}} \simeq \frac{g_{os}}{g_{fs}}$$

$$h_{ob} = \frac{g_{is}g_{os} - g_{fs}g_{rs}}{g_{is} + g_{rs} + g_{fs} + g_{os}} \simeq \frac{g_{is}g_{os}}{g_{fs}} - g_{rs}$$

Common collector paramaters are (common drain)

$$h_{ic} = \frac{1}{g_{is}} \qquad h_{rc} = 1 + \frac{g_{rs}}{g_{is}}$$

$$h_{fc} = -\left(1 + \frac{g_{fs}}{g_{is}}\right) \qquad h_{oc} = \frac{g_{is}g_{os} - g_{fs}g_{rs}}{g_{is}}$$

Using the above common collector paramaters we may calculate the source follower performance.

$$A_v = \frac{-h_{fc}R_L}{h_{ic} + R_L\left(h_{ic}h_{oc} - h_{rc}h_{fc}\right)}$$

where R_L = load resistor in the source lead

$$A_v = \frac{(g_{is} + g_{fs})R_L}{1 + R_L(g_{os} + g_{is} + g_{fs} + g_{rs})}$$

$$A_v \simeq \frac{g_{fs}R_L}{1 + g_{fs}R_L}$$

$$Z_{in} = h_{ic} - \frac{h_{fc}h_{rc}R_L}{1 + h_{oc}R_L}$$

$$Z_{in} = \frac{1}{g_{is}} + \frac{(g_{is} + g_{fs})(g_{is} + g_{rs})R_L}{g_{is}^2 + g_{is}g_{os} - g_{fs}g_{rs}}$$

$$Z_{in} \simeq \frac{1}{g_{is}}$$

$$Z_{out} = \frac{h_{ic} + R_g}{h_{oc}(h_{ic} + R_g) - h_{fc}h_{rc}}$$

where R_g is the source impedance

$$Z_{out} = \frac{1 + R_g g_{is}}{g_{os} + g_{is} + g_{fs} + g_{rs} + R_g(g_{is}g_{os} - g_{fs}g_{rs})}$$

$$Z_{out} = \frac{1 + R_g g_{is}}{g_{fs}(1 - R_g g_{rs})} \simeq \frac{1}{g_{fs}} \quad \text{for } R_g g_{rs} << 1$$

$$\text{current gain} = A_i = \frac{h_{fc}}{1 + h_{oc} R_L}$$

$$A_i = \frac{-(g_{is} + g_{fs})}{g_{is} + (g_{is} g_{os} - g_{fs} g_{rs}) R_L} \simeq -\frac{g_{fs}}{g_{is}}$$

We can also analyze a common source stage with an unbypassed source resistor.

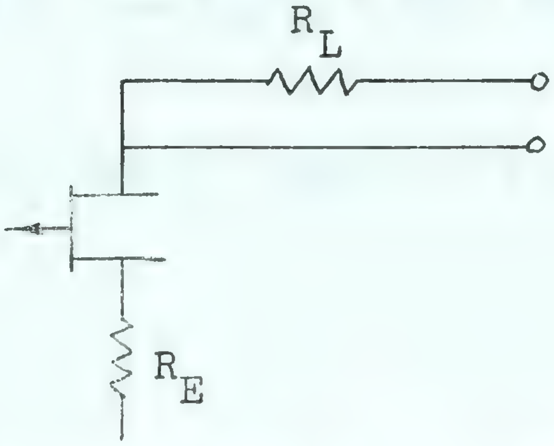


figure I-2 Source Follower with Source Resistor

$$Z_{out} = \frac{1 - h_{rb}}{h_{ob} + \left(h_{ob} + \frac{h_{rb}}{Z_g}\right) \frac{(1 - h_{rb}) h_{fe} - (1 + h_{fe}) h_{ob} R_E}{1 - h_{rb} + (1 + h_{fe}) \left(h_{ob} R_E + \frac{h_{ib} + R_E}{R_g} \right)}}$$

If $\frac{g_{os}}{g_{fs}} \ll 1$ and $\frac{g_{is} g_{os}}{g_{fs}} \ll g_{rs}$

$$Y_{out} = -g_{rs} + \frac{\left(-g_{rs} + \frac{g_{os}}{g_{fs} R_g}\right) \frac{g_{fs}}{g_{is}} \left(1 + g_{rs} R_E\right)}{1 + \frac{g_{fs}}{g_{is}} \left[\left(-g_{rs} + \frac{1}{Z_g}\right) R_E + \frac{1}{g_{fs} R_g} \right]}$$

If also $g_{rs} R_E \ll 1$ and $\frac{1}{R_g} \gg g_{rs}$

$$Y_{out} \simeq -g_{rs} + \left(\frac{g_{os}}{g_{fs} R_g} - g_{rs}\right) \frac{g_{fs} / g_{is}}{1 + \frac{g_{fs} R_E}{g_{is} - R_g} + \frac{1}{g_{is} R_g}} \qquad (5)$$

$$A_v = -G \left(\frac{h_{fe}}{1 + h_{fe}} - \frac{h_{ob} R_E}{1 - h_{rb}} \right) \frac{1 - h_{rb}}{1 + g}$$

where $G = \frac{R_L}{R_E}$ $\qquad$ $g = \frac{h_{ib}}{R_E} + Gh_{ob}R_E + G\left(\frac{h_{fe}h_{rb}}{(1+ h_{fe}} + \frac{h_{ib}h_{ob}}{1 - h_{rb}}\right)$

If $\frac{g_{fs}}{g_{is}} \gg 1$ and $\frac{g_{os}}{g_{fs}} \ll 1$

$$A_v \simeq \frac{- R_L/R_E\left[1+ g_{rs}R_E\right]}{1+ \frac{1}{g_{fs}R_E} + R_L/R_E\left[- g_{rs}R_E + g_{os}/g_{fs} - g_{rs}/g_{fs}\right]}$$

With normal values of R_L and R_E this can be approximated very closely by:

$$A_v = - \frac{R_L}{R_E}\,\frac{g_{fs}R_E}{1+ g_{fs}R_E} \qquad (6)$$

Appendix II

Compound Connected Field Effect Transistor

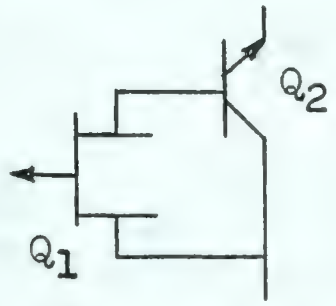


figure II- 1 FET Compound

Edwards(4) has shown that a compound connected pair of transistors can be considered as a single transistor with h-paramaters as given below.

With the approximations

$$h_{fe_2} \gg 1 \qquad\qquad h_{rb_2} \ll 1$$

$$h'_{ie} = B\left[\frac{h_{ib_1}}{h_{fe_2}} + h_{ib_2}\left[\frac{h_{ob_1}h_{ib_1}}{1-h_{rb_1}} + \frac{h_{fe_1}}{1+h_{fe_1}}\,h_{rb_1}\right]\right]$$

$$h'_{re} = B\left[\frac{h_{ob_1}h_{ib_1}}{1-h_{rb_1}} - \frac{h_{rb_1}}{1+h_{fe_1}}\right]\left[\frac{1}{h_{fe_2}} - h_{ob_2}h_{ib_2}\right]$$

$$h'_{fe} = \frac{h_{fe_1}h_{fe_2}}{1+\dfrac{1+h_{fe_1}}{1-h_{rb_1}}\,h_{fe_2}h_{ob_1}h_{ib_2}}$$

$$h'_{oe} = B\left[h_{ob_1} + \frac{1-h_{rb_1}}{1+h_{fe_1}}\,h_{ob_2}\right]$$

$$\text{where } B = \frac{\dfrac{1+h_{fe_1}}{1-h_{rb_1}}\,h_{fe_2}}{1+\dfrac{1+h_{fe_1}}{1-h_{rb_1}}\,h_{fe_2}h_{ob_1}h_{ib_2}}$$

If we now use the paramater conversions of

Appendix I and make the further approximations

$$\frac{g_{fs}}{g_{is}} \ll 1 \qquad \text{and} \qquad \frac{g_{os}}{g_{fs}} \ll 1$$

$$\text{then } B = \frac{\frac{g_{fs}}{g_{is}} h_{fe2}}{1 + h_{fe2}h_{ib2}\left[g_{os} - \frac{g_{fs}}{g_{is}} \quad g_{rs}\right]}$$

$$\text{and } h'_{ie} = \frac{1}{g_{is}} + h_{fe2}h_{ib2}\left[\frac{g_{os}}{g_{fs}} + \frac{g_{os}}{g_{is}} - \frac{g_{rs}}{g_{is}}\right]$$

$$\simeq \frac{1}{g_{is}}$$

$$h'_{re} = -\frac{g_{rs}}{g_{is}}\left[1 - h_{fe2}h_{ob2}h_{ib2}\right]$$

$$\simeq -\frac{g_{rs}}{g_{is}}$$

$$h'_{fe} = \frac{\frac{g_{fs}}{g_{is}} h_{fe2}}{1 + h_{fe2}h_{ib2}\left[g_{os} - \frac{g_{rs}g_{fs}}{g_{is}}\right]}$$

$$\simeq \frac{g_{fs}}{g_{is}} h_{fe2}$$

$$h'_{oe} = h_{fe2}\left[g_{os} - \frac{g_{fs}g_{rs}}{g_{is}} + h_{ob2}\right]$$

These may now be converted to common source y- paramaters.

$$g'_{is} = \frac{1}{h'_{ie}} = g_{is} \tag{1}$$

$$g'_{fs} = \frac{h'_{fe}}{h'_{ie}} = g_{fs}h_{fe2} \tag{2}$$

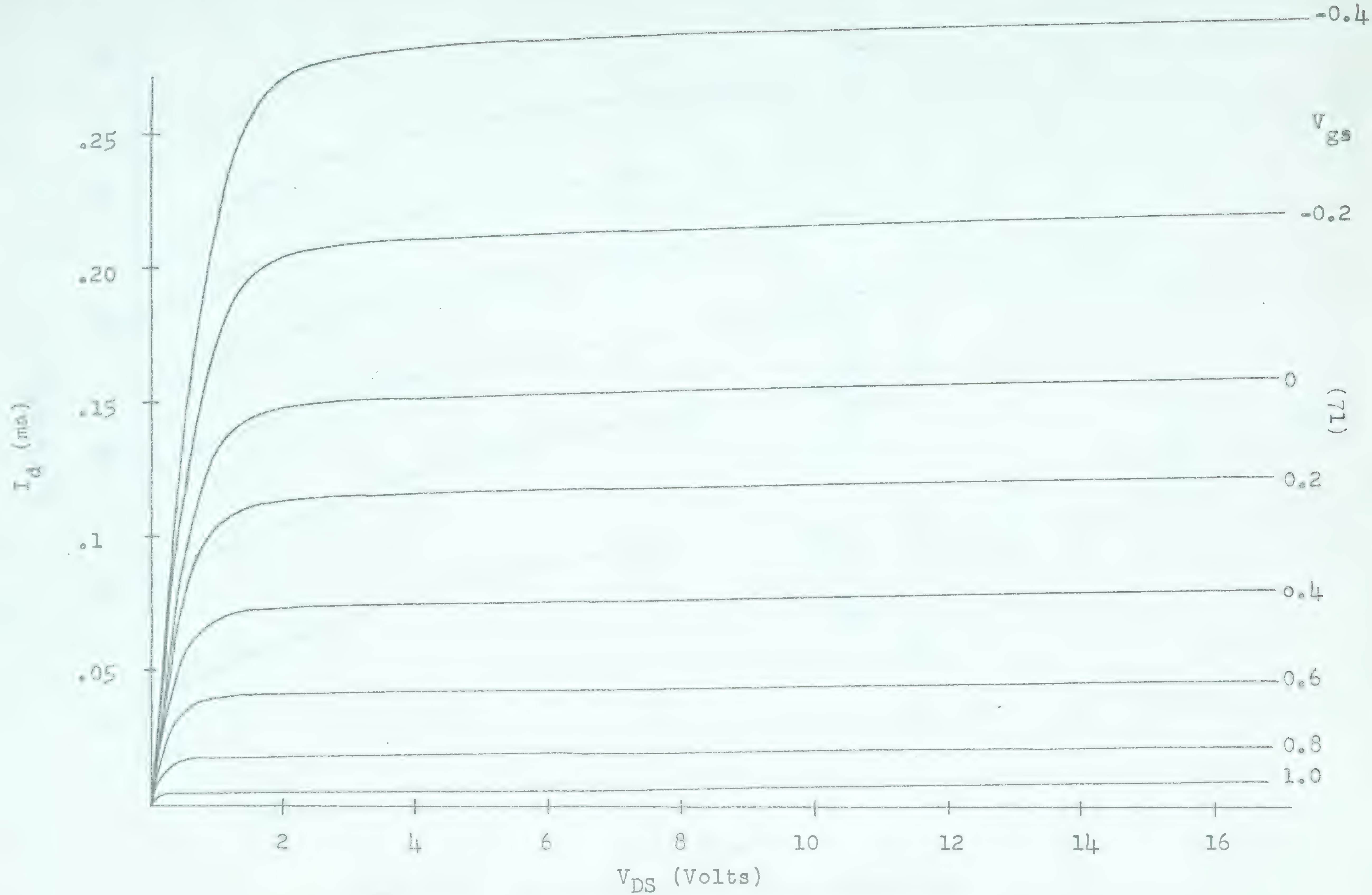
$$g'_{rs} = -\frac{h'_{re}}{h'_{ie}} = g_{rs} \tag{3}$$

$$g'_{os} = \frac{h'_{ie}h'_{oe} - h'_{re}h'_{fe}}{h'_{ie}}$$

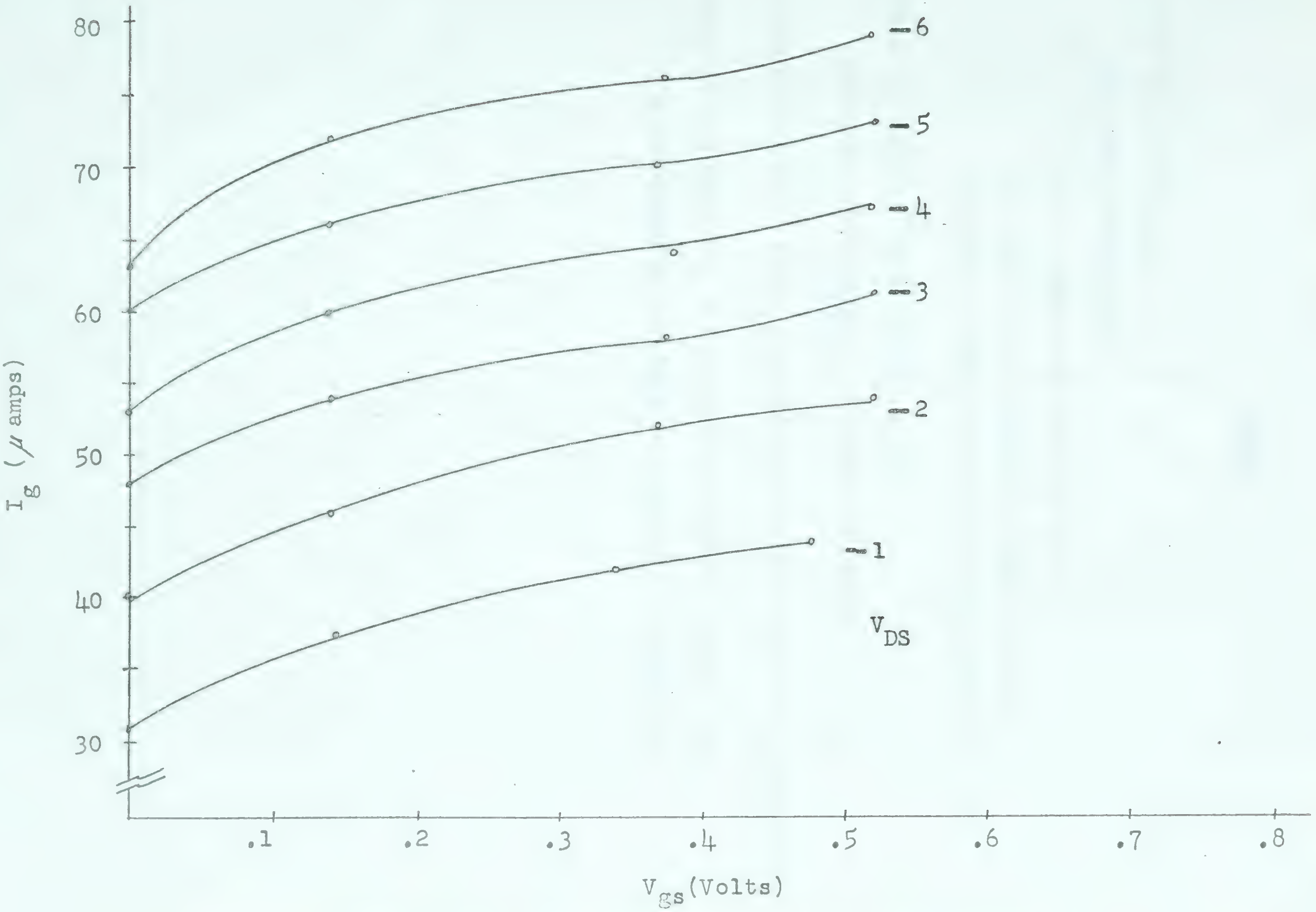
$$= h_{fe2}\,(g_{os} + h_{ob2}) \tag{4}$$

Appendix III

The two graphs shown in this appendix give the characteristics of the 2N2842 transistor used in the amplifier of Chapter III.



Graph III-1 Drain Characteristics of 2N2842 FET



Graph III-2 Input Characteristics of 2N2842 FET

ERRATA

1) Page 17 should read:

and the system will

- a) be maximally flat if $\gamma = 0$
- b) have a low frequency boost if $\gamma < 0$
- c) have a reduced low frequency gain if $\gamma > 0$

2) Page 33 the 10th line should read:

pico-amp was desired. In order to reduce ....

3) Page 58 the 21st line, the word milenated should be myelinated.

4) Page 20 and Page 37, definition of symbols should read:

k = Boltzmann's constant = $1.374\mathrm{x}10^{-23}$ joule/°K.